TVE 08 006
Examensarbete 30 hp
April 2008

High Speed Electronics for Free Space Optical Communication between Spacecraft

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Abstract

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This master thesis mainly covers the electronic design, manufacturing and testing of an FSO (Free Space Optics) communication system intended for a data transfer speed of at least 1 Gbit/s. The system is intended to be used in space to transfer data between satellites in clusters, up to a few kilometres apart, and should be designed with commercially available fiber optic electronics. The usage of commercial off-the-shelf components provides an inexpensive system compared to current space-based FSO systems. The parts of the FSO system constructed in this thesis are electrical-to-optical (high speed transmitter) and optical-to-electrical (high speed receiver) circuit boards. A multiplexing unit (serializer circuit board) is also constructed, that converts several parallel data lines to a high speed data stream. The high speed transmitter is composed of a VCSEL (Vertical Cavity Surface Emitting Laser), a small memory unit and a VCSEL driver whereas the receiver is composed of an avalanche photodiode, a transimpedance amplifier and a limiting amplifier. The serializer circuit board is composed of a clock buffer and a serializer chip. All the designed circuit boards are constructed on double-sided copper laminates and tested with a high speed oscilloscope. The circuit boards designed in this thesis should be seen as a technology demonstration and a prototype of a future integrated system. Much work has been done in this thesis to obtain knowledge about the properties of FSO electronic circuits. The characteristics of VCSELs, APDs and PIN photodiodes are investigated in order to provide a basis for future integrated designs.

This thesis also covers the design, simulation, manufacturing and testing of a low speed transmitter and receiver. The low speed FSO system is based on basic components e.g. operational amplifiers and transistors. Conclusions from these circuit board designs, e.g. knowledge of the steps from idea to complete circuit board, are useful for the high speed design and manufacturing.

This thesis has resulted in three high speed circuit boards and two low speed circuit boards. The three high speed circuit boards reached a data speed higher than 1 Gbit/s.
□
The thesis work has been done in the project OCOM, for the research group ÅSTC, as a course at Uppsala University in Sweden. The thesis completes the degree in Master of Science in Space Engineering, Luleå University of Technology, Sweden.

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TVE 08 006
Sponsor: Rymdstyrelsen, VINNOVA

Contents

1. Introduction

The intended scope of this thesis is to develop and test a high speed free space optic (FSO) communication system. The system should be composed of a laser diode, an APD[i] or a PIN[ii] photodiode. A final system should also incorporate lenses and a pointing system. This FSO system is mainly intended to be used in space by miniature satellites in cluster configuration. Distances between the satellites should be in the range of a few kilometres and the communication speed should be at least 1 Gbit/s. The system is supposed to be manufactured by commercially available fiber optic components. The usage of commercial of the shelf components provides a low-cost system compared to current space-based FSO systems. A great amount of time has been spent in finding, evaluating, selecting and ordering the specific components. This thesis proposes an electronic design and describes the manufacturing and testing of the electronics. It also evaluates the properties of APDs, PINs and VCSEL[iii] (the type of laser diode intended for use), and important parameters are discussed, such as the selection of modulation current. The drawbacks and advantages of using either APD or PIN is evaluated and discussed. The designed high speed system is manufactured and tested and is shown to function as intended. The component selection, along with developed circuit boards, described in the following chapters, should be well suited for the future design of an integrated system.

A subtask in the thesis is to design, build and test a low speed transmitter and receiver based on classical components e.g. BJTs[iv] and operational amplifiers. Important conclusions from this task are useful for the high speed system design and manufacturing, and this subtask is mainly done in order to simplify the high speed system design.

This thesis work is a success and most stated requirements have been fulfilled.

[i] Avalanche Photodiode
[ii] Positive Intrinsic Negative
[iii] Vertical Cavity Surface Emitting Lasers
[iv] Bipolar Junction Transistors

2. Background

2.1. Free Space Optics

Free Space Optics (FSO) has been around in different forms since the late nineteenth century. Essentially all progress in optical communication systems have been made over the last 40 years or so. Most of this progress can be related to military applications. The first example of FSO technology was demonstrated by Alexander Graham Bell, with his invention of the "photophone". This device converted voice sound into telephone signals and transmitted them with a beam of light through free space to a receiver a few hundred meters away. Although the "photophone" never became a commercial reality, Bell considered this his preeminent invention and not the telephone. This was because it did not require a transmission wire. [1]

The only essential requirement for an FSO system to work is that there is a free line of sight between the transmitter and receiver. But generally FSO systems need some kind of free space optic apparatus like telescopes. FSO systems similarly to fiber optic systems use lasers to transmit data. The light beams are transmitted by lasers and focused by lenses and then received by some kind of detector. Standard commercial systems offer speeds in the range of 100 Mbit/s to 2.5 Gbit/s, and demonstration systems have reached speeds up to 160 Gbit/s [1]. Optical data transmission is in most cases done by use of fibers. However, it is possible with the use of almost the same components to transmit the data via free space. One design issue in FSO systems is the need for high precision alignment of the transmitter and receiver. It may be necessary to use automatic feedback for this reason. Because of large loss of power between the transmitter and receiver, particularly for large transmission distances, it is important to focus the energy to the receiver. At the receiver it is not only essential to collect as much power as possible, but also to minimize noise e.g. background light and electrical noise. Noise increases BER[i] and as a result lowers the data transmission capacity. The modulation format also affects the BER. [2]

Compared to other wireless-based transmission technologies like radio waves, FSO is far more secure [1], and the main reason for this is that the narrow laser beam must be intercepted. Because of the short wavelength lasers beam divergence is much smaller than that of a radio or microwave source of similar size. This makes much more of the power transmitted from the sender reach the receiver in FSO compared to longer wavelength technology e.g. radio. However, the loss from the transmitter to the receiver in FSO is in most cases still very large, particularly for large transmission distances. To mitigate this loss of power, it is essential to direct the energy of the sender in the form of a well collimated laser beam. Collimating a diverged laser diode beam can be made with an optical telescope. Because a laser normally has a highly defined wavelength, background light often can be suppressed by use of optical filters. FSO technology is now increasingly used, both on earth and in space. [2]

[i] Bit Error Rate (Described in Appendix D)

2.1.1. Free space optics in space

Satellites and other space vehicles have extensively relied on radio or microwave links to transmit scientific data. However, since the radio spectrum becomes increasingly crowded and the amount of data grows, the development in laser-based communication is exceedingly welcomed by scientists.
Because an FSO system is smaller, more lightweight, is less power-demanding and has a greater bandwidth than an equivalent radio-frequency (RF) system, it is a favourable technology to be used by space vehicles. Other advantages are that laser-based links are not regulated by any restrictions as is the case for RF and that transmission are secure from interception. Given these attractions it is not surprising that FSO is increasingly used in space.
Several important trials have been performed over the past years, including satellite-to-earth and satellite-to-satellite communications.

When operating an FSO system in space environment there are both drawbacks and advantages compared to Earth usage. Some of them are stated below:

- If the communication is "space-to-space" the atmosphere and its weather is no problem that weakens the signal received at the detector.
- The degradation of the driving electronics, lasers and detectors can be a problem in space due to radiation, especially when the system is supposed to be operational over several years.
- The movement of the satellites may misalign the detector and receiver and a space system requires an integrated aligning system.
- For systems operational in space the weight and size is a concern, and thus should be minimized.

The first FSO communication in space was performed in 1992 when the Galileo probe received light pulses from Earth during its flyby. The pulses were received by a solid-state imaging camera.

The Japanese satellite ETS-VI[i] performed a 1 Mbit/s communication experiment with a ground station over the years 1994-1996. However, the satellite was not launched into its planned geostationary orbit (GEO) which made continuous communication hard to maintain.

An optical link between ESA's satellite ARTEMIS[ii] and the French satellite SPOT-4[iii] demonstrated an optical link of 50 Mbit/s over a distance of 30 000 km. This experiment is considered a great success, with a bit-error-rate of less than 10^{-9}. The transmission equipment, carried by SOT-4, SILEX[iv] used an 800 nm semiconductor laser with an output power of 60 mW.

In 2001 a few months before the SILEX experiment, the US satellite GEOLite[v] in GEO demonstrated a successful optical link to earth. However, scientific and

[i] Engineering Test Satellite VI
[ii] Advanced Relay and Technology Mission
[iii] Satellite Probatoire d'Observation de la Terre
[iv] Semiconductor Laser Inter-Satellite Link Experiment
[v] Geosynchronous Lightweight Technology Experiment

technology details have not been made public due to the military nature of the project.

In December 2005 bi-directional optical communication was performed by earth-orbiting satellites. The two satellites communicating was JAXA's[i] OICETS[ii] and ARTEMIS. OICETS in low earth orbit (LEO) and ARTEMIS in geosynchronous earth orbit (GEO).

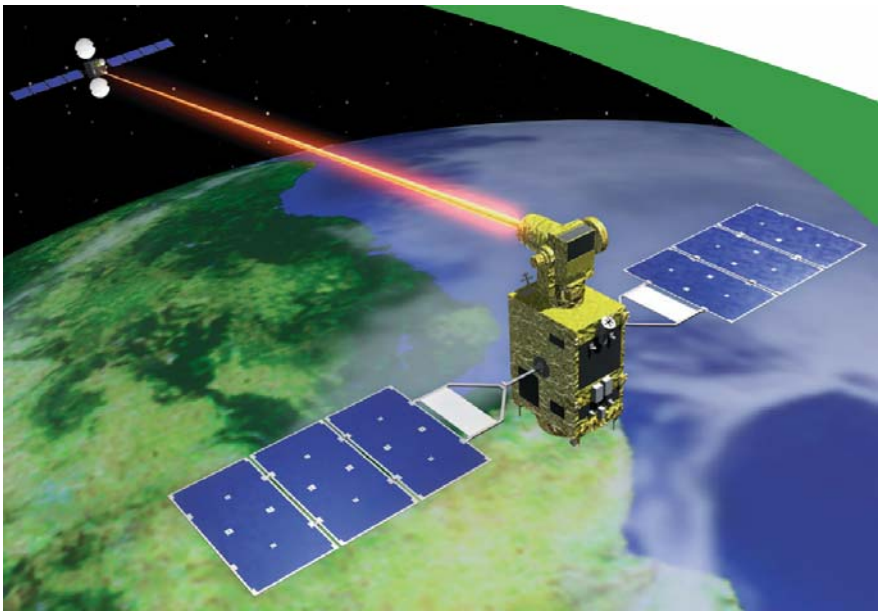

Figure 1: An artist's illustration of ARTEMIS and OICETS. [4]

The communication system used was LUCA[iii], which is a transmitter and receiver utilizing a high power semiconductor laser, a highly sensitive detector and a 25 cm telescope. Because of the large distance (up to 40 000 km) and relative movement of the two satellites an advanced and extremely precise pointing and tracking system, capable of aiming within a few micro radians, had to be used. The mission was a complete success and communication was also performed by OICETS to earth, which is the only optical communication test performed between ground and LEO.

In 2009 NASA plans to launch Mars Telecom Orbiter (MTO). As MTO enters Martian orbit in September 2010 the transmission system will be turned on and then support a 1-30 Mbit/s communication link back to earth. Because of the high power needed to transmit such a vast distance the transmission system, MLCD[iv], is equipped with an amplified fibre laser. This laser will be able to transmit pulses at a peak power of 300 W and an average power of 5 W utilizing the power efficient 64-PPM[v] scheme. The telescope at the end of the transmitter is 30.5 cm in diameter and is carefully isolated against vibrations. MTO will be the first ever deep space laser communication link. [3]

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[i] Japanese aerospace exploration agency's
[ii] Optical Inter-orbit Communications Engineering Test Satellite
[iii] Laser-Utilizing Communications Equipment
[iv] Mars Laser Communication Demonstration system
[v] 64-Pulse Position Modulation

2.2. FSO electronics

The FSO electronics can be divided into a transmitter and a receiver block. The individual blocks which the system in this thesis is based on are described in this section.

2.2.1. Transmitter

An optical transmitter converts an electrical bit sequence to an optical data stream. Because the light output of a laser diode is defined as a function of the input current rather than voltage, laser diodes are driven by currents. Small fluctuations in voltage over the diode would result in dramatic changes in current and light output. An often used type of laser diode in high speed communication is VCSEL. A laser driver can be considered a simple high speed current switch controlled by a modulated data stream at the input. In general, the laser driver is the component determining the maximum speed and overall performance of the transmitter. To control the laser's output power that varies over temperature and over lifetime, some laser driver circuits incorporate a monitoring photodiode (MPD) that provides feedback. Typically, differential input is used and that offer many advantages, as reduced noise and a higher bandwidth. [5] The first step in a transmitter is the serializer which multiplexes several low speed data signals to a single high speed data stream. A serializer is a part in a SERDES[i] device. A block diagram of the transmitter described can be seen in Figure 2 below. [6] Observe that transmitters can be built with other components than described above.

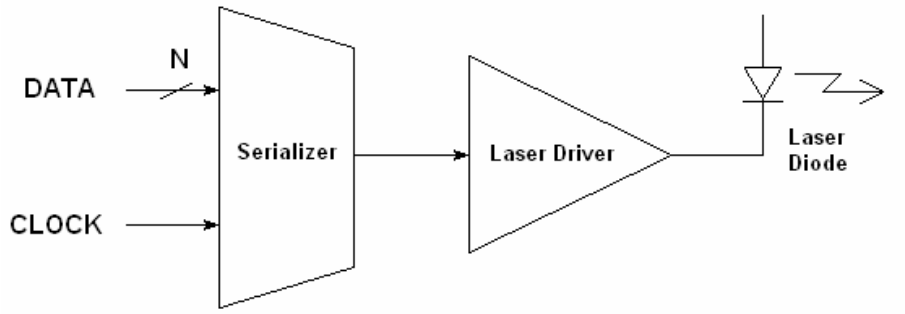

Figure 2: A common optical transmitter design.

2.2.2. Receiver

One of the most critical parts in optical communication systems is the receiver of the optical signal. The receiver mainly determines the total performance because it handles the lowest signal level in the communication link. To convert the optical input signal to an electrical output signal, the most basic receiver consists of some type of photodiode and a transimpedance amplifier (TIA). The photodiode for a high speed system can either consist of a PIN photodiode or Avalanche photodiode. A TIA converts the small photocurrent from the photodiode to a voltage while adding as little noise as possible. The voltage output from the TIA is generally too small to reach a detectable logic level so additional voltage amplification is necessary and thus a limiting amplifier (LA) is connected. A LA has a high gain and a maximum output voltage swing. The input signal is generally always amplified to the maximum output voltage at the rails of

[i] Serializer-Deserializer

the LA. This produces a reasonable constant output voltage swing for a wide range of input signals. If the LA is connected to the TIA by dc-coupling, offset compensation is needed to avoid that the LA saturates at one rail. After the data stream has been amplified to detectable logic levels, noise is removed from the signal and the clock is extracted from the data by the clock and data recovery (CDR) circuit. [7] The CDR also retimes the data to the extracted clock. After the CDR the data is demultiplexed by the deserializer to multiple low speed channels. A deserializer is a part in a SERDES device. [6] The LA and TIA together are generally called the analog front-end of the optical receiver. The block diagram of a receiver can be seen below in Figure 3.

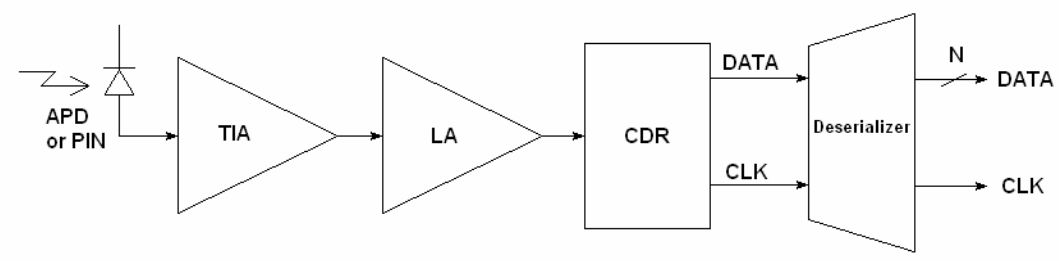

Figure 3: A common optical receiver design.

2.3. Vertical Cavity Surface Emitting Laser (VCSEL)

In 1996 the first commercial device became available but VCSELs have been around in various forms since the late 1970's. Unlike Edge Emitting Lasers (EEL) that emits light horizontally, VCSELs emits light vertically from the surface like an LED. But compared to a LED, a VCSEL usually have a higher output power, a less diverged beam, is more efficient and is much faster. VCSELs are high speed laser diodes ideally suited for high speed data communication in the Gbit/s range. The most common VCSELs are composed of GaAs/AlGaAs and emit light in the range 750-980 nm. However, both longer wavelengths[i] and shorter wavelengths[ii] are available. [8]

Because of the low threshold current and relatively low temperature dependence, VCSELs have excellent jitter[iii] characteristics [9]. VCSELs typically has very low threshold currents and low modulation current requirements. VCSELs produce a circular and low diverged laser beam. They are also relatively stable and in many cases do not need feedback power control or a monitoring photodiode [10].

VCSELs are constructed by depositing up to several hundred thin layers of semiconductor material and subsequent dicing. The light or photon production occurs in the "active region" between two mirrors like in any other laser. Compared to other types of semiconductor lasers the "active region" is very short and the light must pass through the active medium many times to reach enough amplification. This is reached by the relatively high reflectivity of the mirrors. A cross section of a typical VCSEL can be seen in Figure 4. [10]

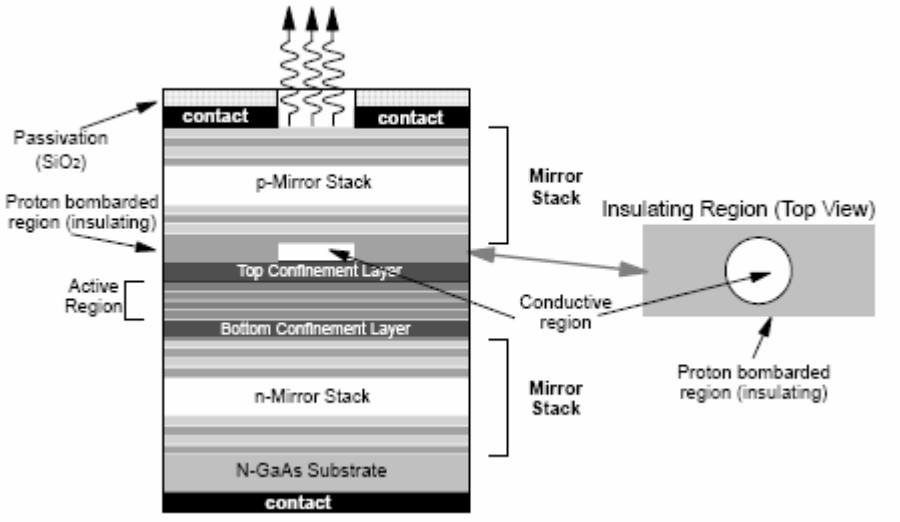

Figure 4: Cross-section of a typical VCSEL. [10]

[i] Typically 1.3 µm, 1.55 µm or beyond 2 µm
[ii] Down to ~650 nm
[iii] Timing error (described in Appendix D).

2.3.1. VCSEL characteristic

In this chapter some important characteristics of VCSELs are described.

2.3.1.1. Threshold current behaviour

Below threshold current the emitted power of a VCSEL is almost zero but above threshold the emitted power varies almost linearly with current. The threshold current of a VCSEL is varying with temperature. For a typical Edge Emitting Laser the threshold current is always increasing with raised temperature but for a VCSEL the threshold current has a parabolic dependence on temperature. This parabolic characteristic (seen in Figure 5) leads to small variations in threshold when the temperature is close to T_0 and larger variations when the temperature is far from T_0. However, the threshold current can vary significantly between actual devices (see Figure 6). [9]

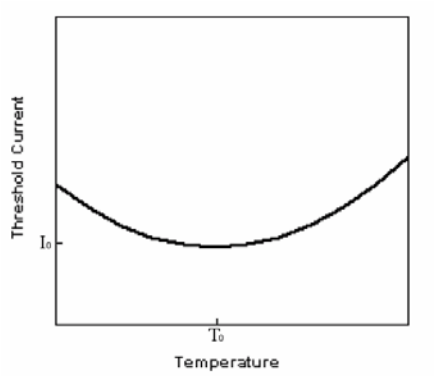

Figure 5: The variation of threshold current with Temperature of a typical VCSEL. [9]

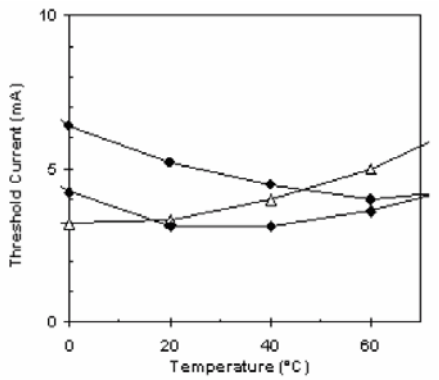

Figure 6: The threshold current of three different devices of the same model. Note that T_0 can vary quite a lot. [9]

2.3.1.2. Slope efficiency behaviour

The change in emitted output power divided by the change in current is defined as the slope efficiency, η i.e. [9]

$$\eta = \frac{\Delta P}{\Delta I}, \tag{2:1}$$

where η is the slope efficiency, P is the emitted output power and I is the current through the device. In general for a VCSEL the slope efficiency decreases approximately linear with temperature (seen in Figure 7). This makes the output power rollover at some current above threshold and maximizes the output power. The rollover current is the point where the output power starts to decrease by increasing current; this point can be seen in Figure 8. The change in slope efficiency is often given in the datasheets at a reference temperature (typically 25 ºC) in the unit of %/ºC or ppm/ºC. A typical value of the slope efficiency is -5000 ppm/ºC. [9]

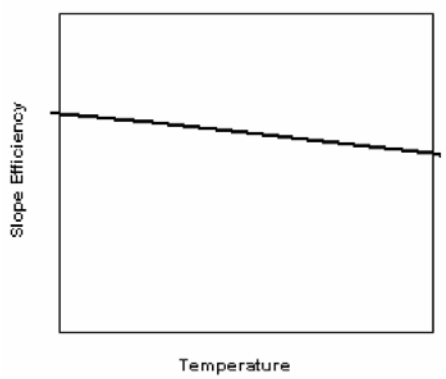

Figure 7: The slope efficiency above threshold. [9]

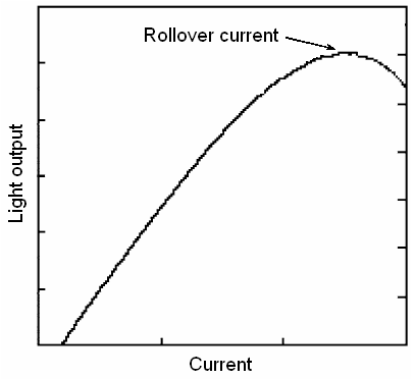

Figure 8: Rollover current.

2.3.1.3. Emitted power behaviour

The emitted power depends both on the driving circuitry and the characteristics of the VCSEL. With a constant current source and a current a few mA below the rollover current the output power can with temperature dependence be approximated as [9]

$$\mathrm{P(I,T)} \approx \eta(T) \cdot \left[I - I_{TH}(T) \right], \tag{2:2}$$

where P is the emitted output power, I the current through the device, I_{TH} the threshold current, T the temperature and η the slope efficiency. An example of the output power versus temperature of a VCSEL is shown in Figure 9.

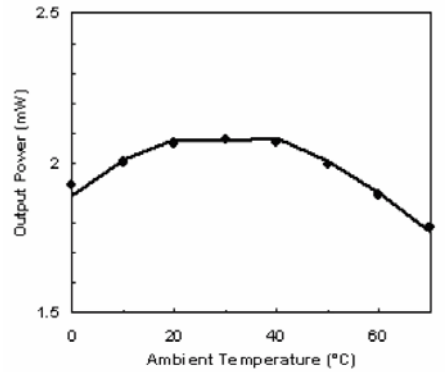

Figure 9: Emitted power of a VCSEL versus the ambient temperature. Observe that the output power is close to constant near 30 ºC. [9]

The emitted power can be maintained with either a positive or negative temperature coefficient or maintained near constant, by suitable selection of the operating point and the temperature coefficients of the driving circuit. There are several ways to make the VCSEL operate at a stable output power versus temperature in an electronic design:

- Operate far above threshold.
- Limit or control the temperature range which the VCSEL operates in.
- Characterize each VCSEL individually and compensate the behaviour exactly to optimize the output power behaviour.
- Control the output power by feedback from the emitted light with a monitoring photodiode (MPD). [9]

2.3.1.4. Reliability behaviour

The reliability of VCSELs is very favourable compared to typical edge-emitting lasers and LEDs. The MTTF[i] of a typical VCSEL operated at moderate currents in room temperature exceeds 10 million hours. The reliability of VCSELs shows a high dependence on temperature and a common rule of thumb is that the lifetime decreases with increased temperature. [9]

2.3.1.5. Relaxation resonance

The relaxation resonance of a laser can produce oscillations at the pulse rising edge and can sometimes be a problem. The relaxation resonance frequency of VCSELs is typically above 5 Gb/s and the amplitude is small so at most typical operating speeds the relaxation resonance can be ignored [9]. But when operating VCSELs at very low modulation and bias currents the relaxation resonance frequency is lower. This is one of the reasons not to operate VCSELs at too low modulation currents, especially when operating close to the threshold current. The low relaxation resonance of VCSELs compared to an Edge-emitting laser is showed in Figure 10. [9]

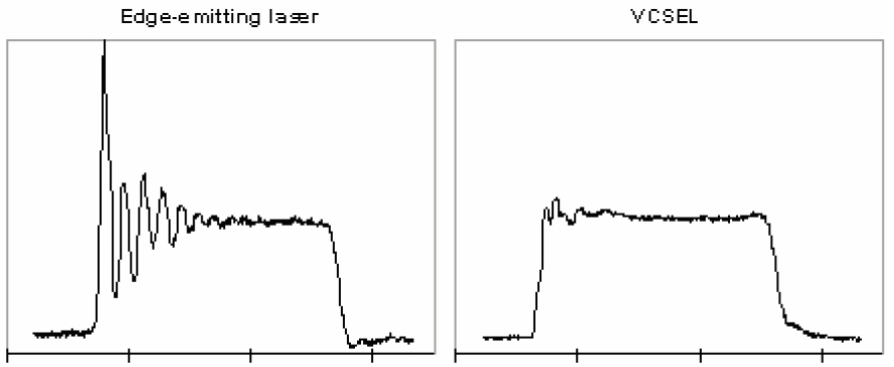

Figure 10: Comparison of an Edge-emitting laser and a VCSEL when affected by relaxation oscillations. The time per step in the scale is 1 ns. [9]

2.3.1.6. Turn on delay

When a VCSEL is operated at a pulse zero level current (I0) well above threshold and a pulse one current level (I1) above that, the optical power follows the rising edge with a delay of just few tens of picoseconds [9]. When lowering I0, the delay at the rising edge is increased. Because delay does not occur at the falling edge, the result is distortion of the pulse width. The turn on delay is dependent on the data transmitted; the data sequence “11100001” gives a higher delay time for the last “one” than “11111101”, this is because “11111101” doesn’t have enough time to reach the zero level at the last “one”. An example of this data dependence is shown in Figure 11. The best way to minimize the turn on delay is to place the pulse zero level above or near threshold**.** [9]

[i] Mean Time To Fail

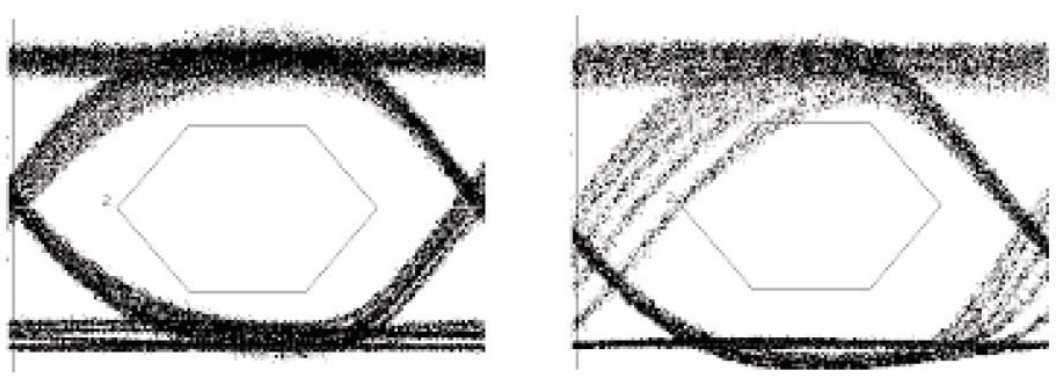

Figure 11: Eye diagram of a signal biased correctly (left) and a signal biased too far below I_{TH} (right). Both signals are K28-5 patterns. [9]

2.3.1.7. Extinction ratio (ER)

Extinction ratio is defined as the ratio of the one level power and the zero level power. One complication is that ER is measured in several different ways (average power, power when the ringing has died out etc.) which thus gives different values of ER. The ER is usually measured in dB and calculated as [9]

$$ER[dB] = 10\log_{10}(P_1 / P_0) \tag{2:3}$$

where P_1 is the power at a one and P_0 is the power at a zero.

2.3.1.8. Driving scheme considerations

To properly balance the design of turn-on delay and ER, it is necessary to balance the VCSEL close to threshold, typically less than 0.5 mA between I_{bias} and I_{TH}. The change of threshold current over temperature has to be taken into account; however the threshold change of many VCSELs does not vary much more than 0.5 mA over a wide temperature spectrum.

A modulation current of less than 4 mA is generally not good because the sensitivity to temperature and lifetime degradation is increased when a small change in threshold is a big fraction of the modulation current. In order to operate a VCSEL at the highest possible speed, a high enough modulation current is required.

Whether a VCSEL is connected directly to the laser driver circuit board or at the end of a transmission line, the mismatch in impedance is usually of great concern. A laser driver is designed with specific output impedance that normally has to be matched with the VCSELs series resistance and the transmission line. If the system is not matched, the current through the VCSEL may suffer from anomalous waveforms that may completely ruin the data signal. An often wise decision is to aim for a mismatch not higher than 10%. Some systems can function at a mismatch higher than 50%, but these are exceptions.

A designed emitter usually must incorporate an allowance in the optical budget to be ensured that the system will be able to operate over the intended lifetime. Depending on the operating conditions and environment, a VCSEL will be degraded over time and the output power will differ. To optimize the optical budget the device-to-device variations must be considered and specific

characteristics of the particular VCSEL device must be measured. Temperature compensation is recommended to achieve significant improvements in the optical budget for temperature variations. [9]

2.3.1.9. Mean Power Control (MPC)

MPC controls by definition the mean optical output power from the laser. The purpose of MPC is to easily eliminate the aging and environmental factors from the optical link budget. To acquire the mean power from the VCSEL, usually a MPD[i] is connected as feedback. MPC can be done by adjusting the bias current, modulation current or both. Because a VCSELs output power is usually dominated by change in slope efficiency and not by variations in threshold current; control of optical output power by adjusting the modulation current (or both) is usually the best choice. The shortcoming of MPC is that when it changes the current to control the optical power, the time delay and extinction ratio is changed [9]. This is of great concern for the performance of an optical link. Figure 12 demonstrates the behaviour of a VCSEL incorporating MPC by adjusting the modulation current. Observe that no temperature compensation is used, which may increase the performance greatly.

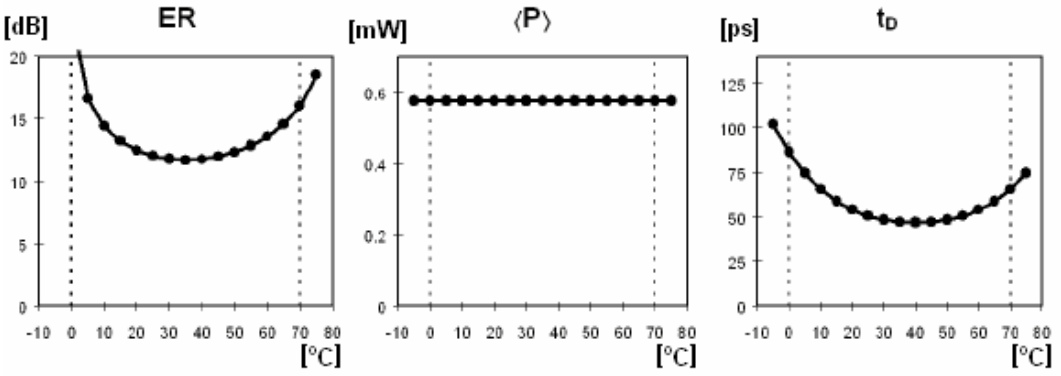

Figure 12: Extinction ratio, mean power and time delay when the optical output power is controlled by adjusting the modulation current of a VCSEL. [9]

When open loop operation is utilized no feedback of the VCSEL is used. The benefit by incorporating a circuit of this type is the simplicity. Temperature compensation is possible in open loop operation and can be used in the circuit to achieve better performance. The disadvantage of this kind of customization is that the output power of the VCSEL will never be known and thus the optical budget must be customized for each individual VCSEL. [9]

[i] Monitoring photodiode

2.4. Photodiodes

Photodiodes are light sensitive semiconductors that are manufactured in almost the same way as "normal" semiconductor diodes. The primary difference is that photodiode chips are larger and they are packaged to allow light to slip into the diode. When a photon of sufficient energy strikes the diode, an electron is excited and thus a mobile electron and a positively charged "hole" are created. If this occurs in or close to the junction's depletion region, the carriers are swept from the junction by the built-in field, or the reverse voltage field, of the depletion region. The holes move toward the anode, and electrons toward the cathode, and a photocurrent is produced [11]. The best detector of choice in a high speed communication system is a PIN[i] photodiode or an avalanche photodiode. The "normal" PN[ii] photodiode is much to slow to be operated in high speed communication.

Photodiodes are typically constructed of one of the three materials Si, Ge or InGaAs, but other materials can be used (GaAlAs, GaAs, InGaAs, Ge, InGaAS, and InP) [12]. All of these materials have different properties and one of the most significant differences is the spectral responsivity (seen in Figure 13 and described in section 2.4.3.1). The main parameters of the three materials mostly used are shown in Table 1.

Table 1: Typical characteristics of Si, Ge and InGaAs. [12]

Parameter	Si	Ge	InGaAs
Wavelength (nm)	300-1100	500-1800	1000-1700
Peak response (nm)	800	1550	1700
Peak responsivity (A/W)	0.5	0.7	0.9
Dark current (nA)	1	200	10
Typical risetime (ps)	500	100	300

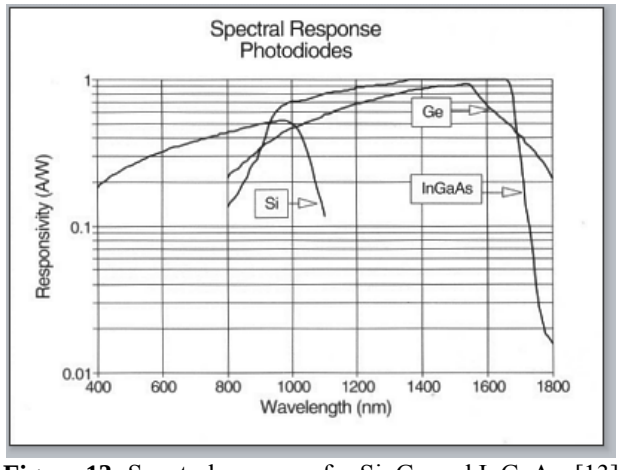

Figure 13: Spectral response for Si, Ge and InGaAs. [13]

[i] Positive Intrinsic Negative
[ii] Positive Negative

2.4.1. PIN photodiodes (PINs)

Because of the extremely thin depletion layer, PN photodiodes is much too slow to be used for high speed optical communication. For PIN photodiodes the response time i.e. frequency response has been improved by extending the PN-junction[i] with a very lightly n-doped[ii] layer called the intrinsic layer. The intrinsic layer acts as a very wide depletion region that decreases capacitance and favours current carriage by drift (faster than diffusion), thus increasing the speed of the device [10]. The response time can be further improved by increasing the reverse voltage. However, increasing the reverse voltage also increases the dark current[iii] [14]. One more improvement with an intrinsic layer is that it acts as a volume that absorbs photons; this increases the sensitivity[iv] [10]. A cross-section of a typical PIN photodiode can be seen in Figure 14. Electron-hole pairs are created by incident photons in the intrinsic layer and separated by a reverse voltage to create a current (photo current) through the diode. The PIN photodiode must be reverse biased to function and the strength of the reverse bias extends the depletion region which increases the sensitivity of the PIN photodiode [14].

Because of the favourable properties described above, ordinary PIN photodiodes are used in nearly all infrared optical links at present.

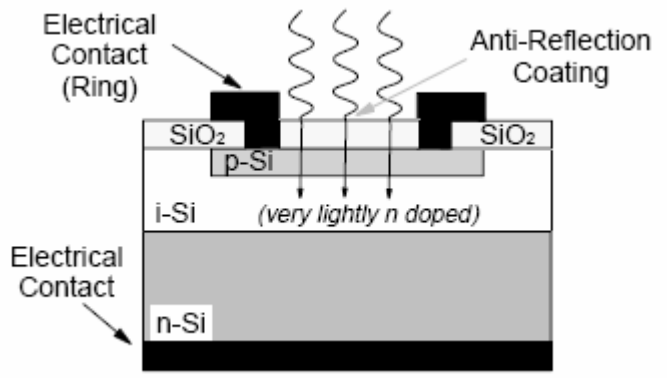

Figure 14: Cross-section of a typical PIN photodiode. [10]

[i] Boundary between the positive and negative layer
[ii] Negative doped
[iii] described in section 2.4.3.2
[iv] described in section 2.4.3.1

2.4.2. Avalanche photodiodes (APDs)

An APD is basically an extremely sensitive PIN operated at a very high reverse voltage. PIN photodiodes are typically biased at a few volts but APDs generally have a reverse bias of 50 volts or more. This high reverse voltage generates an internal gain (avalanche multiplication) and a higher reverse voltage results in a higher gain. This makes the APD very sensitive and APDs are generally used where sensitivity is more important than other factors. A negative effect of increasing the reverse voltage is that the dark current is increased. One weakness of the avalanche photodiode is that the gain is strongly temperature dependent. This means that the gain in some applications needs to be stabilized by feedback or that the temperature needs to be controlled. The main structural difference between an APD and a PIN is that the PINs i-layer[i] is lightly p-doped and renamed to the π-layer in the APD. The π-layer is also typically thicker than the i-layer. A cross section of a typical APD structure can be seen in Figure 16. [10]

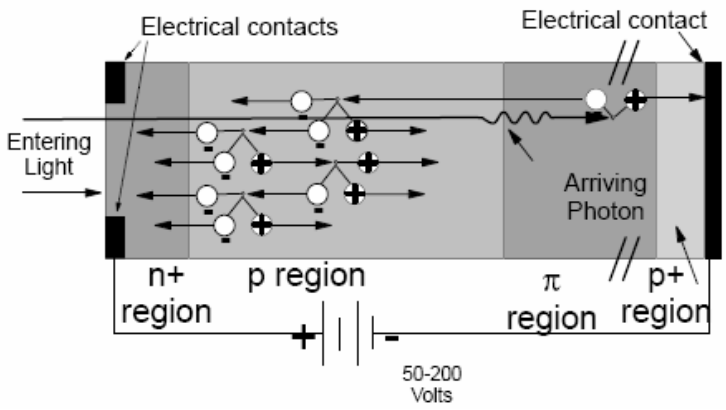

Figure 15: The multiplication process in an APD. Be aware that the multiplication region (p region) has been greatly enlarged to show the avalanche process. [10]

An APD operates in the following way (as can be seen in Figure 15):

- A photon passes through the thin n+ and p-region, is absorbed in the π-layer and an electron-hole pair is created.
- The electrical field in the π-region accelerates the electrons and holes. The strength of the electrical field can be seen in Figure 17.
- When the free electron from the π-region comes close to the p to n+-junction, the very strong electric field accelerates the electron to such a high speed that impact ionization occur.
- The newly created electrons and holes from the impact ionization are accelerated themselves and may collide again and create new electron-hole pairs. This process is called avalanche multiplication.

The result of the process described above is that a single photon can result in hundreds of created electron-hole pairs.

[i] intrinsic layer (lightly n-doped)

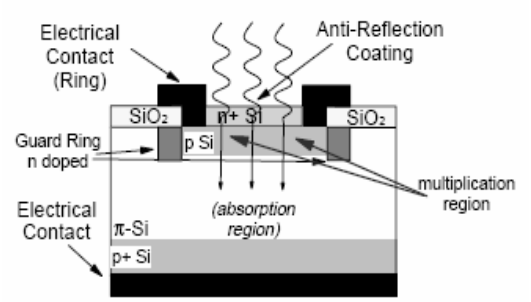

Figure 16: Cross-section of a typical avalanche photodiode. [10]

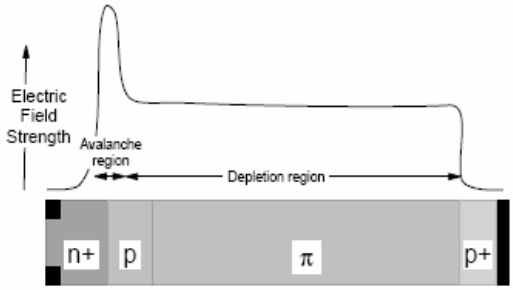

Figure 17: The electric field in an APD. [10]

The response time of the APD is, much like the PIN, characterised by the junction capacitance. However, because an avalanche can last quite a long time, the "Avalanche Build-up Time" can limit the APDs maximum speed [10]. APDs are generally noisier than PINs because electron-hole pairs created by ambient heat are amplified by the avalanche process. One disadvantage of using APDs instead of PINs is that the random nature of the internal gain increases the variance of the generated photocurrent [12]. The power consumption of an APD is generally much higher than for a PIN photodiode [20].

Some APDs are able to operate in Geiger mode[i]. This makes the APDs sensitive enough to be used for single photon detection. In Geiger mode the signal current must be limited not to damage the APD.

[i] above breakdown voltage

2.4.3. Photodiode characteristic

In this chapter the most important photodiode characteristic are described. The effect on APDs and PINs to radiation environment can be found in appendix C.

2.4.3.1. Spectral response

Spectral response is a measurement of how effective a photodiode transforms incident light to current and it is strongly dependent on the wavelength of the photons. Two ways to characterise spectral response are photo sensitivity and quantum efficiency. For a "normal" photodiode increasing the reverse voltage changes the spectral response characteristics slightly. The spectral response of an APD is highly dependent on the gain. If a low reverse voltage is applied the spectral response characteristics is almost the same as for "normal" photodiodes.

The ratio of photocurrent produced by a photodiode (in short-circuit) divided by the incident light at a given wavelength, is expressed as the photo sensitivity (S) or responsivity. S is either expressed in the amount of amperes produced per input power of light (A/W) or as a relative value normalized for the peak sensitivity. If S is normalized, then it is expressed as a percent (%). S is calculated at a given wavelength as [18]

$$S(\lambda) = \frac{I_P}{P}, \tag{2:4}$$

where $S(\lambda)$ is the photo sensitivity at wavelength λ, I_P is the photocurrent and P is the incident optical power.

Quantum efficiency (QE) is similar to photo sensitivity and is commonly expressed in percent (%). The QE is the amount of holes or electrons that contribute to the photocurrent per incident photon.

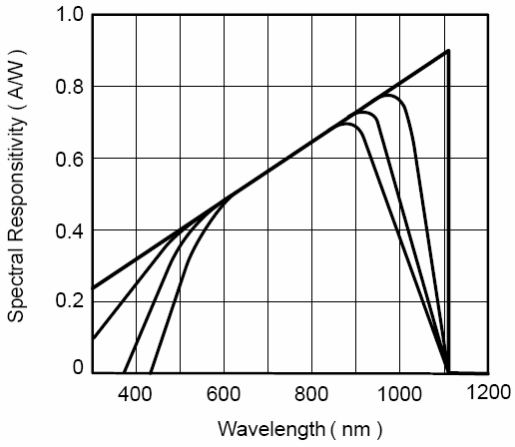

Figure 18: The responsivity of several typical Si photodiodes and the ideal value (straight line). [18]

The sensitive area or sensitive volume is the active part of the detector where incident photons results in a measurable photocurrent. The photo sensitivity depends on the photodiode material, applied reverse bias and temperature. With the exception of the APD, an increase of the applied reverse bias increases S slightly due to improved charge collection in the photodiode. Increase of reverse

bias for an APD increases S considerably. When the temperature is increased the band gap between the valence band and the conduction band is decreased and longer wavelength photons are able to excite electrons and thus contribute to the photocurrent. In other words increased temperature increases the photo sensitivity at longer wavelengths [20]. For shorter wavelengths (<600 nm) reduced photo sensitivity is observed with increasing temperature due to increasing recombination rates close to the surface. However, the photo sensitivities temperature behaviour at short wavelengths cannot be generalized [18].

2.4.3.2. Dark current

When photodiodes are connected with a reverse voltage a small leakage current (dark current) flows through the photodiode even if no light enters the active area. This current is the main source of noise and is present in photoconductive (reverse bias) mode of operation. Dark current shows strong exponential temperature dependence and is approximately doubled for every 8-10ºC temperature increase [8 and 13]. The exact change of dark current over temperature is affected by several parameters such as thickness of the substrate, resistivity and reverse voltage and thus the dark current can vary considerably between different photodiode types. [18 and 20]

For an APD the dark current are dependent on the gain and follows the equation [21]

$$I_D = I_{ds} + M \cdot I_{dg}\,, \tag{2:5}$$

where M is the gain, I_{ds} the surface leakage current flowing between the PN junction and Si oxide layer and I_{dg} is the internal current generated inside the Si substrate.

2.4.3.3. The Gain (M) of APDs

The gain of an APD is a strong function of the reverse voltage and temperature, and it is defined as the output current at the applied reverse voltage divided by the output current at low reverse voltage. An increase in the reverse voltage normally increases the gain. However, because of the internal resistance and the photocurrent flowing through the device, a voltage drop occurs when furthering increasing the reverse voltage and this causes the gain to decrease [21]. The gain versus reverse voltage for different temperatures is shown in Figure 19.

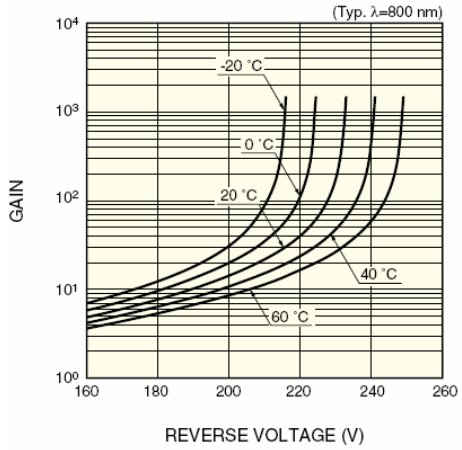

Figure 19: The gain for different temperatures versus reverse voltage for the Hamamatsu APD, S6045. [22]

In many applications a constant gain is important and the reverse voltage must be controlled by feedback with respect to the temperature, or the temperature must be held constant. The temperature coefficient is commonly expressed in %/ºC or V/ºC. [21]

If the device is operated beyond the breakdown reverse voltage, damage may result to the device. For single photon detection operation, the APD is operated beyond the breakdown voltage (Geiger mode).

For an APD, the SNR[i] can be improved by increasing the gain. If the surface leakage current (I_{ds}) can be ignored, the gain to obtain the maximum SNR for APDs (M_{Opt}) is calculated by the following formula [21]

$$M_{Opt} = \left[\frac{4k_B T}{q\left(I_p + I_{dg}\right)R_L x} \right]^{\frac{1}{2+x}} \qquad (2:6)$$

where R_L is the load resistance, x is the excess noise index and I_{dg} is is the internal current generated inside the Si substrate.

2.4.3.4. Terminal Capacitance of PINs

The product of the terminal (or junction) capacitance and the external load resistor is the main factor determining the response time of a photodiode. The terminal capacitance is formed in the depletion region and the capacitance is directly proportional to the width of the depletion region and the diffused area. By increasing the reverse bias, the width of the depletion region increases and thus lowering the junction capacitance. Further increase of the reverse voltage will only decrease the capacitance up to the point where the depletion region expands to the back surface of the photodiode chip; at this point the capacitance becomes nearly constant.
[20]

[i] Signal-to-Noise Ratio

2.4.3.5. Terminal capacitance of APDs

APDs have the same terminal capacitance characteristics as normal photodiodes. Because carriers produced outside the depletion layer may cause problems such as slow decay time, a fast response time is ensured by increasing the reverse voltage up to the point (or higher) of constant terminal capacitance. A high enough reverse voltage causes the thickness of the depletion layer to be wider than the penetration depth of light and thus no carriers are produced outside the depletion layer. [21]

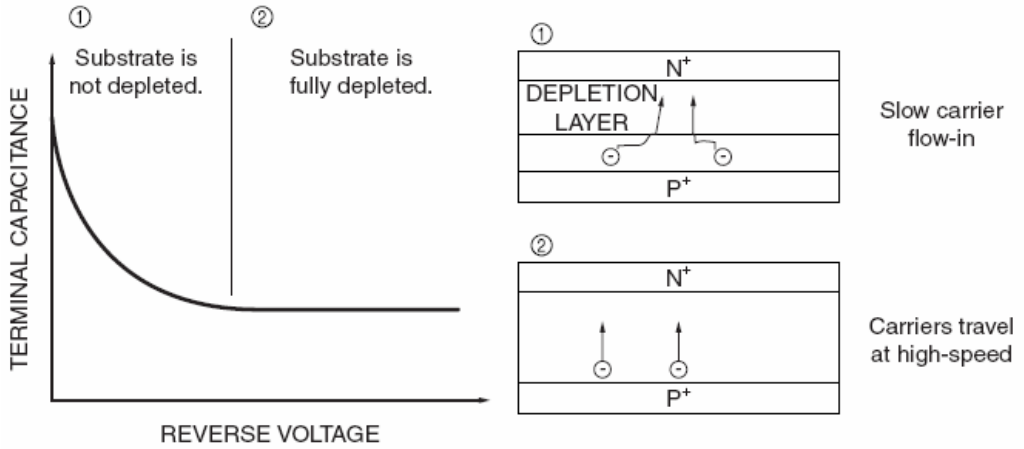

Figure 20: Operating APDs in region 2, ensures a high response speed, due to no carrier production outside the depletion region. [21]

2.4.3.6. Connecting an APD to a circuit

APDs can be handled and connected to a circuit as normal photodiodes; the only exception is that a high reverse voltage must be used. However, some precautions should be taken. To protect the APD from overheating a protective resistor or a current limit circuit should be connected to the circuit. Because of the high reverse voltage biasing the APD, excessive voltage over the readout circuit may occur if the readout circuit has high input impedance. To prevent this, a protective circuit should be connected. When using an APD over a wide temperature range, it may be necessary to control the temperature of the APD or to use feedback controlled bias voltage. [20]

2.5. A Transimpedance amplifier

Transimpedance amplifiers convert the small photo current from a photodiode to a measurable voltage. A low component count and simple TIA can be seen in Figure 21. The low speed receiver in section 3.1.4 is based on this circuit. The difference between the low speed receiver and circuit in Figure 21 is just that the photodiode is biased differently. Due to the capacitance of the photodiode (C_D in Figure 22) the typical TIA is prone to oscillate. To guarantee stability the feedback capacitor must be set to a specific value. [23]

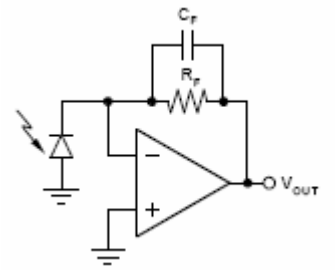

Figure 21: Typical TIA with photodiode. [23]

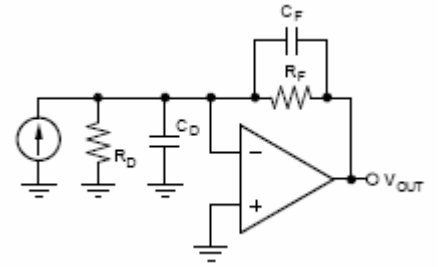

Figure 22: Typical TIA with photodiode modelled by ideal elements. [23]

The ideal transimpedance transfer function of the TIA in Figure 21, is [23]

$$V_{OUT} = -I_S Z_F = -I_S \frac{R_F}{1 + j2\pi f R_F C_F} \tag{2:7}$$

The appropriate feedback capacitor for stability can be calculated by [23]

$$C_F = \frac{1}{4\pi R_F GBW}\left[1 + \sqrt{\left(1 + 8\pi R_F C_D{}' GBW\right)}\right] \tag{2:8}$$

where R_F is the feedback resistor, $C_D{}'$ is the sum of the input capacitance at the negative input of the op amp and the terminal capacitance (C_D, described in section 2.4.3.4) of the photodiode. GBW is the gain-bandwidth product.

3. Low speed system

3.1. Design and methods

3.1.1. Overview

The main goal of the low speed system is to design, manufacture and test a low speed FSO system, based on basic components e.g. op amps and transistors. No specific minimum requirements are set, just that it should be capable of transmitting and receiving optical signals. The design and manufacturing has resulted in two circuit boards:

- Low speed transmitter
- Low speed receiver

The low speed transmitter makes the electrical to optical transformation and the high speed receiver makes the optical to electrical transformation.

3.1.2. Component selection

A number of components at different manufacturers were browsed and a selection of components was ordered, some of these are used in the designed circuit boards. The selection of the components to the low speed circuit boards is based on the following characteristics:

- The availability of specific components; some components could only be ordered in great numbers. This limited the selection of components. Many components used in the thesis are possible to sample free.
- The detectors responsivity[i] at the laser's wavelength must be sufficiently high.
- Components easy to solder are preferable.

Below is a short description of all individual components used on the designed low speed circuit boards.

Optowell's **PH85-F1P0S2**[ii] is a high power VCSEL. The laser emits 10 mW[iii] light at 850 nm and is constructed to be used in FSO up to 1.25 Gbit/s [24]. This laser is very hazardous for the eyes and laser protecting goggles should be used.

The PIN photodiode used is Hamamatsu's **S9055**. This detector has a very low terminal capacitance (below 1 pF) and a cut-off frequency of 1.5 GHz[iv]. The active area diameter of the chip is 0.2 mm and the peak sensitivity is 0.4 A/W at 700 nm.

[i] Described in section 2.4.3.1
[ii] PH85 for short in the rest of the thesis
[iii] At 20 mA and 25 ºC
[iv] Typical value at 25 ºC

The op amps[i], **MAX4305** and **MAX4304**, are incorporated in the low speed transmitter and receiver. These two op amps are part of the same series and have similar characteristics. The package used in the designs is 5-pin SOT23.

A BJT of model **2N2222A**, packaged in a 3-pin TO18, is used in the low speed transmitter. This transistor is of NPN type and is designed for high speed switching.

3.1.3. Low speed transmitter

The low speed transmitter mainly consists of an op amp, a BJT (Bipolar Junction Transistor) and a VCSEL. The op amp used is Maxim's MAX4305, the BJT used is STMicroelectronics 2N2222A and the VCSEL is the PH85-F1P0S2. The main idea of the circuit is to function as a constant current source switched on and off by an external pulse generator. When the supply (V_{CC}) is high enough, the current through the laser diode will be dependent on the size of the resistor ($R_{Emitter}$), the voltage applied to the positive port of the op amp and the maximum output swing of the op amp. The simplified schematic of the circuit is shown in Figure 23 and the top and bottom side layout is shown in Figure 24, Figure A - 7 and Figure A - 8.

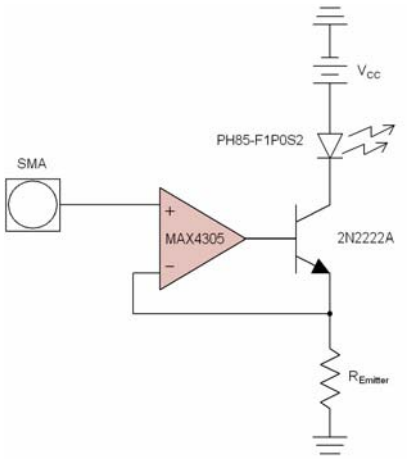

Figure 23: Simplified schematic of the low speed transmitter. In the complete circuit board capacitors are added.

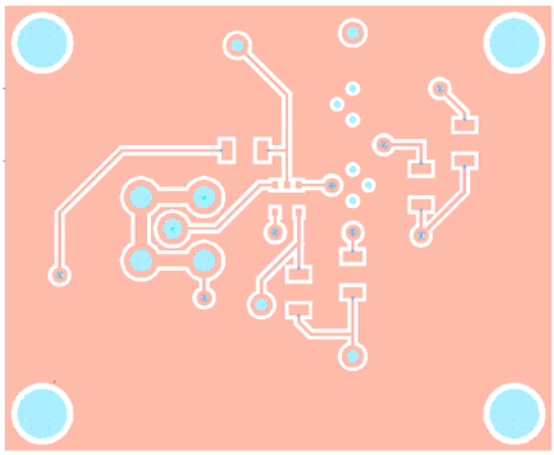

Figure 24: Top side layout of the low speed transmitter.

- The positive and negative supply to the MAX4305 is decoupled with 0.1 µF capacitors.
- The V_{CC} source is decoupled with a 10 µF capacitor.
- A decoupling capacitor to ground of 80 pF is connected between the VCSEL and BJT. This capacitor is placed to minimize the spikes present in the simulation (section 3.2).
- A copper circuit board is used with two layers (top and bottom). The bottom layer is used as ground plane and the top layer is kept floating. All components are placed on the top layer.
- Each via hole has a diameter of 0.6 mm and each via pad a diameter of 1.3 mm on each side (front- and backside).

[i] Operational Amplifier

- To connect the front- and backside of the vias, a short trace is soldered through each via.
- The SMA connector is placed on the bottom layer and the laser placed on the top layer (for easy placement close to a detector).
- $R_{Emitter}$ is set to 150Ω.
- The BJT is packaged in a 3-pin TO18.
- The MAX4305 is packaged in a 5-pin SOT23.
- The 4 mm holes placed in the corners makes it possible to attach the circuit board to a measurement set-up for proper alignment to a receiver when testing.
- An extra pin is soldered between the BJT and $R_{Emitter}$ to simplify measurement of the voltage over the resistor (and thus calculate the current).

In the text below the electrical characteristics of the circuit is described:

Because the op amp keeps the negative input and the positive input at the same voltage level and because the current into the base of the BJT is small, the current through the laser can be expressed as

$$I_{Laser} \approx \frac{V_{in}}{R_{Emitter}}. \quad (3:1)$$

However, because of the maximum output swing of the op amp is ~3.7 volts (found in the datasheet), the maximum voltage at the base ($V_{Base\text{-}Max}$) is ~3.7 volts. The maximum voltage at the emitter ($V_{Emitter\text{-}Max}$) can then be expressed as

$$V_{Emitter-Max} \approx V_{Base-Max} - 0.7\,\text{V} = 3\,\text{V}. \quad (3:2)$$

where 0.7 V is the typical voltage drop from the base to the emitter of a BJT. The maximum current through the laser can then be expressed as

$$I_{Laser-Max} \approx \frac{V_{Emitter-Max}}{R_{Emitter}} \approx \frac{V_{base-Max} - 0.7V}{R_{Emitter}}, \quad (3:3)$$

The current through the BJT and through the laser diode can never float backwards, so putting it all together the current through the laser can be described by the three formulas

$$I_{Laser} = I_{Laser-Max} \approx \frac{3V}{R_{Emitter}}, \text{ if } V_{in} > 3\,\text{V}, \quad (3:4)$$

$$I_{Laser} \approx \frac{V_{in}}{R_{Emitter}}, \text{ if } 0\,\text{V} < V_{in} < 3\,\text{V} \quad (3:5)$$

and

$$I_{Laser} \approx 0, \text{ if } V_{in} < 0\,\text{V}. \quad (3:6)$$

In the manufactured circuit board an emitter resistor ($R_{Emitter}$) of 150 Ω is used. This gives a maximum laser current ($I_{Laser\text{-}Max}$) of approximately

$$I_{Laser-Max} \approx \frac{3V}{150\Omega} = 20\,\text{mA}. \tag{3:7}$$

3.1.4. Low speed receiver

3.1.4.1. Overall design

The low speed receiver consists of an op amp (MAX4304) and a Hamamatsu produced Si PIN photodiode (S9055). The schematic and layout of the circuit can be seen in Figure 25 and Figure 26. The gain and optimum value (for no oscillations) of C_F is approximated in section 3.1.4.2. The circuit and layout of the design is described below.

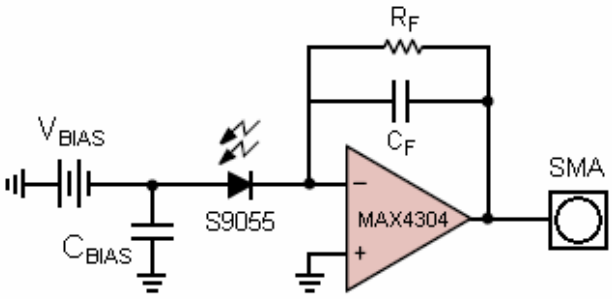

Figure 25: Schematic of the low speed receiver. The supply and the decoupling capacitors to the op amp are not shown.

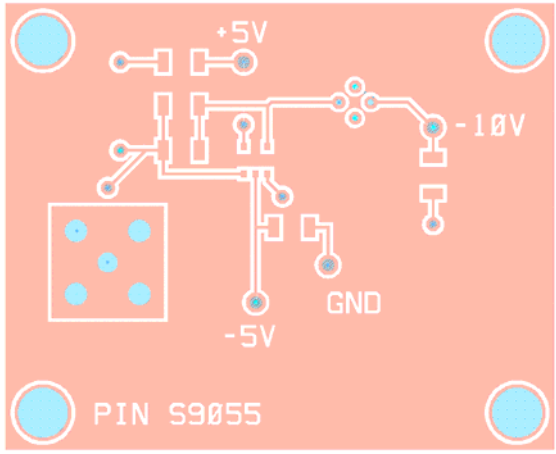

Figure 26: Top layer layout of the low speed receiver.

- A copper circuit board is used with two layers (top and bottom). The bottom layer is used as ground plane and the top layer is kept at floating potential. All components are placed on the top layer.
- R_F is selected to 10 kΩ, C_F selected to 10 pF and C_{BIAS} to 0.1 µF.
- The size of the feedback resistor (R_F) determines the transimpedance (described in 2.5.
- To stabilize the step response at the output, a feedback capacitor (C_F) is connected. The size of this capacitor is essential to obtain a good step response (described in 2.5). The capacitor size calculated is not used in the design. The oscillations can be seen in the circuit test (section 3.3.3).
- To reduce noise from V_{BIAS} a 0.1 µF decoupling capacitor (C_{BIAS}) is connected to the circuit board.
- The op amp used is Maxim's MAX4304 in 5-pin SOT23 package.
- The supply for the op amp is decoupled with 0.1 µF capacitors.
- The S9055 is biased with -10 volts at the anode (V_{BIAS} = 10V).
- The SMA is connected on the top layer.
- Each via hole has a diameter of 0.6 mm and each via pad a diameter of 1.2 mm on each side (front- and backside).
- To connect the front- and backside of the vias, a short trace is soldered trough each via.
- The width of the traces is 0.25 mm.
- The PIN photodiode (S9055) is packaged in a 3-pin TO18.
- An extra hole in the layout is placed for the S9055 footprint. This makes it possible to choose if the photodiode should be placed with top side on top or bottom layer.

- The MAX4304 is packaged in a 5-pin SOT23.
- The 4 mm holes placed in the corners makes it possible to attach the circuit board to a measurement set-up for proper alignment to a receiver when testing.

3.1.4.2. Transimpedance and feedback capacitor

The transimpedance and feedback capacitor's optimum value (for minimum oscillations) are calculated in this section. The formulas from section 2.5 are used.

For the op amp MAX4304, the GBW [i] is 730 MHz [25] and the input capacitance (C_{OP}) is unfortunately unknown (not found in the MAX4304's datasheet). The terminal capacitance (described in section 2.4.3.4) of the s9055 PIN photodiode is 0.8 pF.

For the low speed receiver the appropriate feedback capacitor, to maximize stability, can be approximated by

$$C_F = \frac{1}{4\pi R_F GBW}\left[1+\sqrt{\left(1+8\pi R_F C_D{}' GBW\right)}\right]. \quad (3:8)$$

With $C_D = C_D{}' = 0.8$ pF (ignoring C_{OP}), GBW = 730 MHz and $R_F = 10\ \text{k}\Omega$, the feedback capacitor should be close to

$$C_F = 4.2\,\text{nF}. \quad (3:9)$$

Because the input capacitance of the MAX4304 is not found in its datasheet, the feedback capacitor can not be calculated exactly. By making a guess and setting the input capacitance to 2 pF (as the op amp LT1812), the feedback capacitor can be approximated to

$$C_F = 7.8\,\text{nF}. \quad (3:10)$$

Observe that in the low speed receiver design, the feedback capacitor was set to another value (10 pF) than the optimal one. This is because no calculation was made before the time of completion of the circuit.

The transimpedance of the circuit (described in section 2.5) can be calculated by the formula

$$V_{OUT} = -I_S Z_F = -I_S \frac{R_F}{1+j2\pi f R_F C_F} \quad (3:11)$$

For low frequencies the transimpedance will be close to

$$V_{OUT} = -I_S Z_F = -I_S \frac{R_F}{1+j2\pi f R_F C_F} \approx -I_S R_F \Leftrightarrow -\frac{V_{OUT}}{I_S} \approx R_F = 10\,\text{k}\Omega. \quad (3:12)$$

[i] Gain Bandwidth Product

3.2. Simulations

3.2.1. Low speed transmitter

Simulation of the low speed transmitter with a bit sequence voltage source applied to the input. Models of the op amp (MAX4305) and the BJT (2N2222A) are used. The simulated circuit is shown in Figure 27. Simulation with both PM67 and PH85 are made.

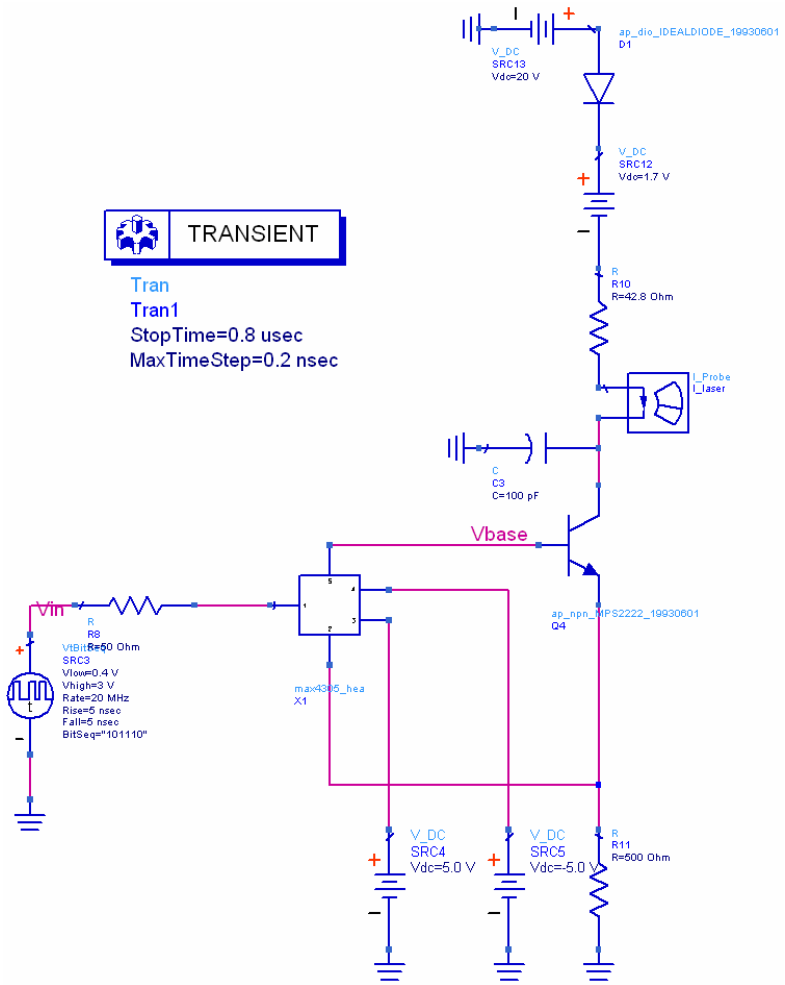

Figure 27: Simulated circuit in Agilent's ADS[i]. The square "block" in the centre is the op amp MAX4305. The measurement instrument connected to the BJT collector is a current probe.

3.2.1.1. Transmitter with the VCSEL PM67

In this test the PM67 is set as laser diode model. The results of the test can be seen in Figure 28 to Figure 30. In this simulation the following parameters are set:

- The emitter resistor ($R_{Emitter}$ in Figure 23) is set to 500Ω.
- The source's frequency is set to 20 MHz and the bit sequence is set to 101110.
- The source is set to switch between 0.4 and 3.0 volts and thus give a switched current (calculated by formula (3:5)) through the VCSEL between 0.8 mA and 6 mA.

[i] Advanced Design System

- The PM67 model (Appendix F) is connected at the collector in series.
- The time step used in the simulation is 0.2 ns.
- The voltage source at the diode's anode is set to 20 volts.

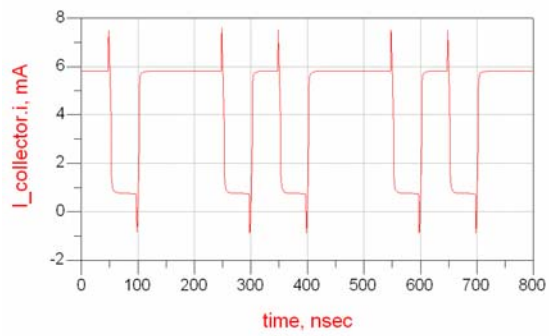

Figure 28: Laser current through the PM67. The source's rise and fall times is set to 5 ns. The 100 pF capacitor at the collector of the BJT is not connected**.**

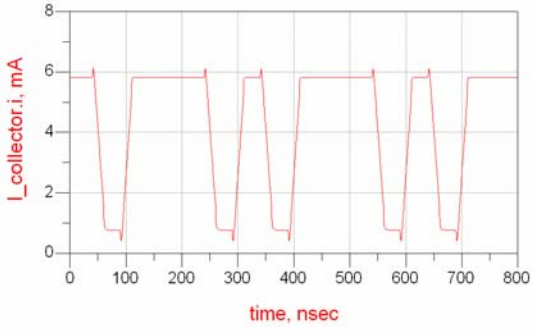

Figure 29: Laser current through the PM67. The source's rise and fall times is set to 20 ns. The 100 pF capacitor at the collector of the BJT is not connected**.**

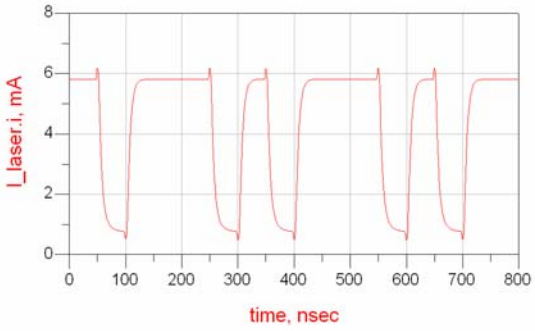

Figure 30: Laser current through the PM67. The source's rise and fall times is set to 5 ns. The 100 pF capacitor at the collector of the BJT is connected.

3.2.1.2. Transmitter with the VCSEL PH85

The results of the test can be seen in Figure 31 to Figure 33. In this simulation the parameters were set as in simulation 1 with the following exceptions:

- $R_{Emitter}$ was set to 150Ω and the current (calculated by formula (3:5)) through the VCSEL will switch between ~20 mA and ~2.7 mA.
- The PH85 model (Appendix F) is connected at the collector in series.

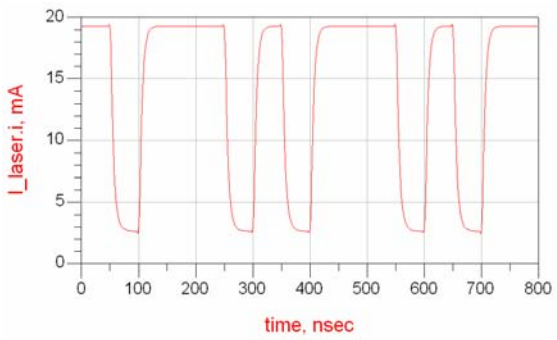

Figure 31: Laser current through the PH85. The source's rise and fall times is set to 5 ns. The 100 pF capacitor at the collector of the BJT is connected.

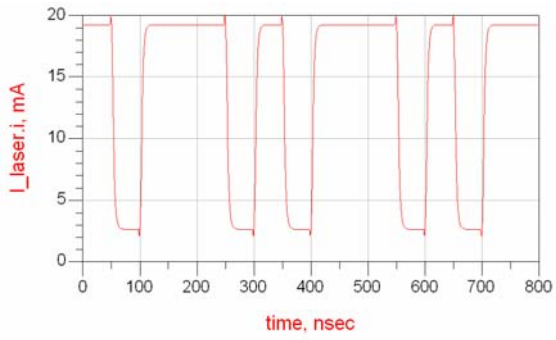

Figure 32: Laser current through the PH85. The source's rise and fall times is set to 5 ns. The 100 pF capacitor at the collector of the BJT is exchanged to 50 pF.

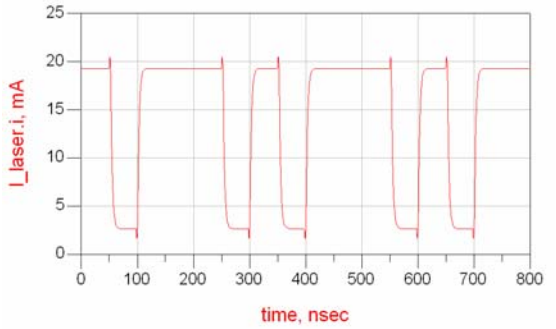

Figure 33: Laser current through the PH85. The bit sequence source is set to 0.4 and 5 volts. Rise and fall times set to 5 ns. The 100 pF capacitor at the collector of the BJT is exchanged to 50 pF.

3.3. Test results

3.3.1. PM5705 Pulse generator

The pulse generator used in some of the tests is Philips PM5705. This pulse generator has a selectable maximum and minimum output level and can generate a square signal up to 10 MHz. The PM5705 does not generate a perfect square wave signal when operating at frequencies close to the maximum frequency. At a frequency of about ~5 MHz the output is distorted and a "ringing" output signal is obtained. At frequencies up to 1 MHz the output signal is very stable with no visible ringing when looking at the whole signal. An output signal from the PM5705 is shown in Figure 34. The PM5705 has selectable high and low output voltages and a constant high and low output (TTL mode). The TTL mode of the PM5705 has a high value of 4.0 volts and a low value of -0.2 volts.

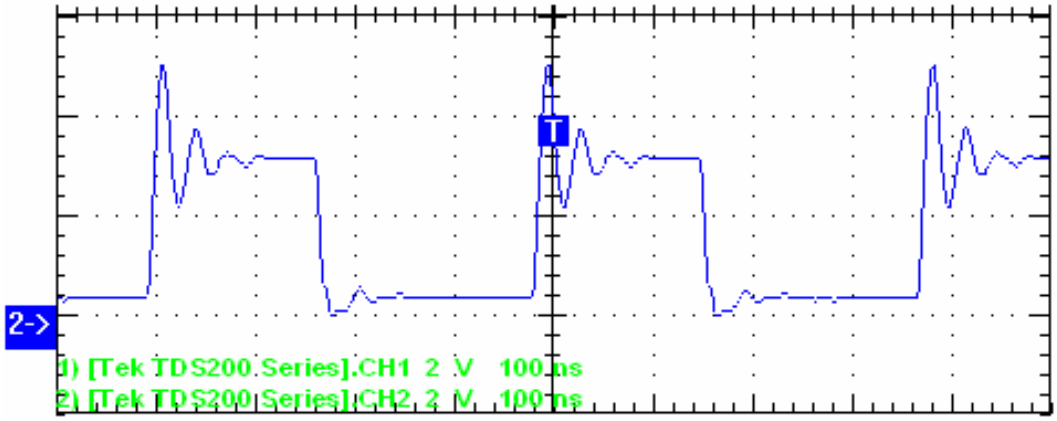

Figure 34: Output signal from the PM5705 when measured by the oscilloscope Tektronix TDS200. 100 ns/line and 2 volts/line.

3.3.2. Low speed transmitter

To test the current through the VCSEL (PH85) the voltage over $R_{Emitter}$ is measured when using the pulse generator PM5705 as input. The test is setup in the following way:

- The square wave generator PM5705 is connected by a 50 Ohm coaxial cable to the input of the low speed transmitter.
- The output is measured with the oscilloscope (Tektronix TDS200) connected by coaxial.
- The input signal is measured.
- V_{CC} in Figure 23 is set to 15 volts.
- The supply of the op amp is set to ±5 volts.

The test results are shown below in Figure 35 and Figure 36. As can be seen in Figure 36 the maximum output voltage over the emitter resistor ($R_{Emitter}$) is approximately 3.4 volts (even if the input voltage is higher (~4 volts)). By using (3:3) the maximum current through the VCSEL ($I_{Laser\ Max}$) is approximately

$$I_{VCSEL\ Max} \approx \frac{3.4V}{150\Omega} = 23\,\text{mA}. \qquad (3:13)$$

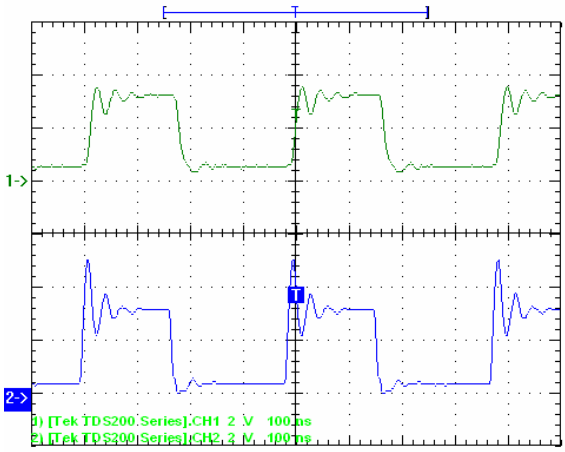

Figure 35: The input signal below and the output signal above. The signal is averaged by the oscilloscope. 100 ns/line and 2 V/line

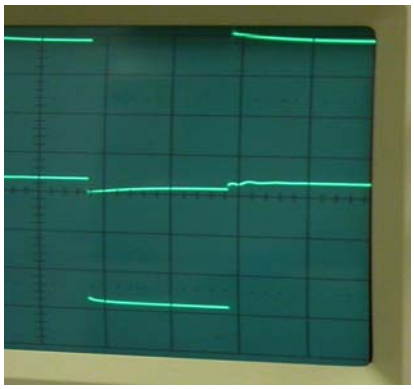

Figure 36: The input signal above and the output signal below. 10 µs/line and 1 V/line. The input signals ground is the centre line and the output signals ground is three steps below the centre.

3.3.3. Optical link between transmitter and receiver

In this section an optical link test between the low speed transmitter and the low speed receiver is described. The test result is shown in Figure 38 and Figure 39. The test is setup in the following way:

- The VCSEL and PIN is aligned as straight as possible toward each other and at a distance of ~1 cm, as can be seen in Figure 37.
- The pulse generator PM5705 is used as input to the low speed transmitter.
- The output signal is inspected by a 20 MHz oscilloscope (LG's OS5020) via a coaxial cable.
- V_{CC} in Figure 23 is set to 15 volts.
- The supply of the op amp is set to ±5 volts.

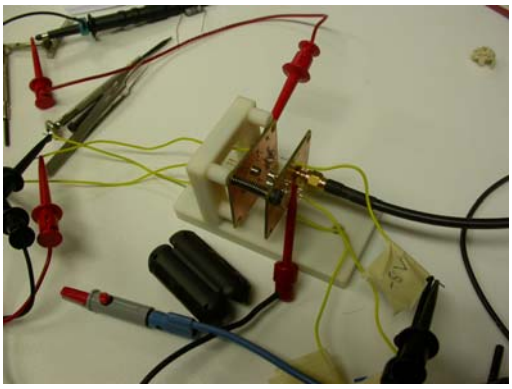

Figure 37: Low speed receiver and low speed transmitter in test fixture.

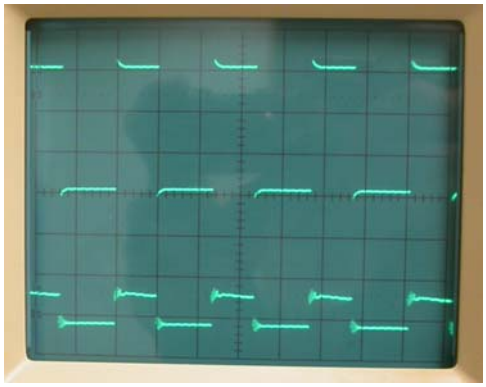

Figure 38: Above, the input signal to the low speed transmitter and below, the output signal from the low speed receiver. The scale is 0.1 ms/line, 1.0 V/line for the top signal and 0.1 V/square for the bottom signal.

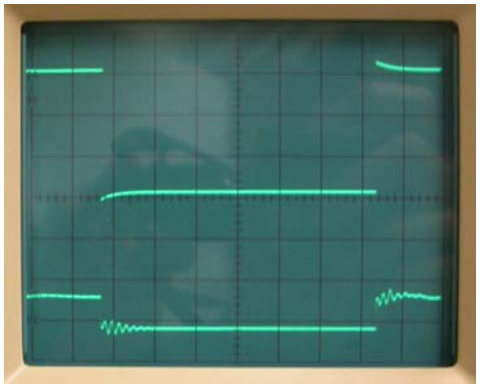

Figure 39: The input signal to the low speed transmitter (top) and the output signal from the low speed receiver (bottom). The scale is 20 µs/line, 1.0 V/line (top signal) and 0.1 V/line (bottom signal).

4. High speed system

4.1. Design and methods

4.1.1. Overview

The main goal of this thesis is to design, manufacture and test a high speed FSO system, based on components used in fiber optics, capable of transmitting and receiving data at a speed of at least 1 Gbit/s. This goal has resulted in three high speed circuit boards:

- Serializer circuit board
- High speed transmitter
- High speed receiver

The high speed transmitter makes the electrical to optical transformation and the high speed receiver makes the optical to electrical transformation. The serializer circuit board multiplexes 10 parallel signals to a high speed signal, sent to the high speed transmitter. These circuit boards are based on the following components/blocks – serializer, VCSEL driver, VCSEL, APD, TIA and LA. All of which are designed to operate together at a speed of at least 1.0 Gbit/s. Block diagrams and the main setup of the high speed circuit boards can be seen in Figure 40 and Figure 42. The clock circuit is not constructed in this thesis; an evaluation circuit board from Lattice is used.

4.1.2. Component selection

The method to decide which individual components to use in each block is described in this section. A number of components at different manufacturers were browsed and a selection of components was ordered, some of these are used in the designed circuit boards. All components used on the high speed and low speed circuit boards are described in section 4.1.3. The selection of the components for the circuit boards is based on the following characteristics:

- The availability of specific components; some components could only be ordered in great numbers. This limited the selection of components. Many components used in the thesis are possible to sample free.
- The detectors responsivity[i] at the laser's wavelength must be sufficiently high.
- Components easy to solder are preferable.
- The data speed of the components must reach at least 1 Gbit/s
- The minimum data speed should preferable be as low as possible, so testing of the circuit boards with low speed testing equipment is possible. This is desirable because if the manufactured circuit board does not reach 1 Gbit/s it might reach a lower speed which can be seen as a small success. The drawback of selecting wide bandwidth components is that it might be more sensitive to noise, compared to low bandwidth components.
- It is an advantage if the components do not require a lot of "extra" components and thus can function on there own. An example of this is that

[i] Described in section 2.4.3.1

some laser drivers require external potentiometers[i] to control parameters such as bias current.
- The components and circuit boards must be able to function together. An example of this is that the voltage levels of the TIA's output must be compatible with the voltage levels of the LA's input. Another example is that the laser driver's bias and modulation current must be compatible with the VCSEL.
- A parameter that the component selection is based on is the input and output impedance. All of the components used in the high speed circuit boards have input and output impedance of 50 Ohms. This makes circuit design easier and component count lower, due to no requirement of termination resistors.
- Specific characteristics like jitter, noise, power requirement, temperature range etc.
- Components with a maximum data speed much higher than 1 Gbit/s is not preferable, due to the increase of noise with bandwidth.

4.1.3. Blocks and Components

In this section a short description of all individual components used on the designed high speed circuit boards are made.

The laser driver selected for use in the high speed transmitter (seen in Figure 40) is Linear Technology's **LTC5100 VCSEL driver**. This component has a wide bandwidth[ii] which gives the advantage to test the transmitter at a lower (and also higher) speed than 1 Gbit/s. The bias and modulation current of LTC5100 can be tuned by an on board I^2C[iii] memory unit, a microprocessor or a computer. At least 128 bits of memory capacity is required and thus a 128 bit EEPROM is selected. Specific factors, like temperature compensation and fault handling, can be programmed on the VCSEL driver. A program (LTC5100 Evaluation Software) downloadable from Linear's homepage (www.linear.com) is an excellent software for setup these parameters. The chip has an internal temperature sensor. The laser can be remotely located connected by a coaxial cable, but in the thesis design it has been placed directly on the circuit board. The on-chip DACs[iv] eliminate the requirement of external potentiometers and the inputs are internally AC-coupled. This simplifies circuit board manufacturing and minimizes size.

The memory unit used in the high speed transmitter is Microchip's **24LC00**. This is a non-volatile 128 bits EEPROM[v]. The term non-volatile means that the stored information is retained even when the circuit is not powered. As package the 8-PIN PDIP is used. The EEPROM is programmed by use of ELNEC's programmer PikProg2.

[i] Variable resistors
[ii] 155 Mbit/s – 3.2 Gbit/s
[iii] I^2C stands for inter-integrated circuit and is a multi-master serial computer bus. It uses only two bidirectional lines, Serial Data (SDA) and Serial Clock (SCL).
[iv] Digital-To-Analog Converters
[v] Electrically Erasable Programmable Read-Only Memory

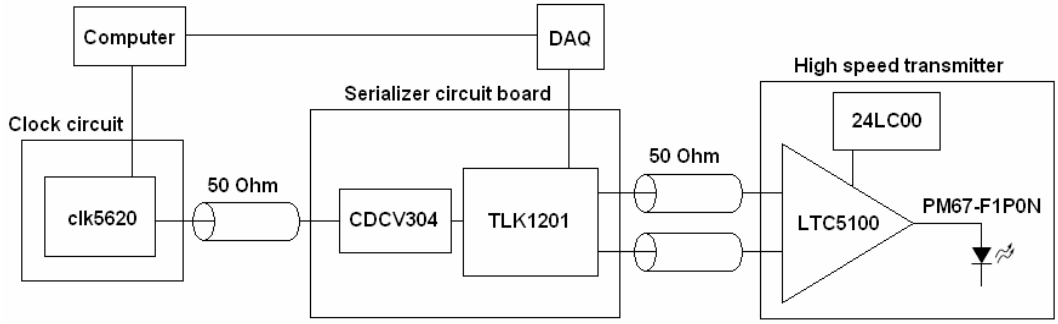

Figure 40: Components and circuit boards on the high speed transmitting side.

The component selected to the serializer circuit board is the **SERDES** device **TLK1201AIRCP**[i]. This device can be operated in full duplex and have on the serializer part 10 input bits and a differential output. In the thesis only the transmitting part of the SERDES is implemented and thus the deserializer is not described. The minimum data rate is 0.6 Gbit/s and the maximum is 1.3 Gbit/s. The device supports two operating modes TBI[ii] and 5-bit interface DDR[iii]. When operating in TBI the device accepts a 10-bit wide 8b/10b parallel word transmitting the code (with a small time delay of 19-20 bits) sequentially from bit 0 to bit 9. The data is transmitted on the rising edge of the clock signal. In DDR mode the device accepts 5-bit wide 8b/10b encoded data and clocks the data on both the rising and falling edge of the clock signal. Bits 0-4 are clocked on the rising edge and bits 5-9 on the falling edge. The data is then sent as a 10-bit wide word with bit 0 transmitted first. The input reference clock (60-130 MHz in TBI) from an external source is internally multiplied by 10 and this multiplied clock is used to register the input data.

The digital out of the **DAQ**[iv] (Agilent's U2356A) is used to set and control the 10 input ports to the TLK1201. The DAQ (seen in Figure 41) has 24 digital output ports that can be controlled by the bundled software Agilent Measurement Manager.

Figure 41: Agilent's Data acquisitioner U2356A. [26]

Texas instruments 140 MHz clock buffer **CDCV304** is connected on the serializer circuit board. This clock buffer is connected to minimize noise and thus produce a better clock signal into the serializer.

[i] TLK1201 or TLK1201AI for in rest of the thesis
[ii] 10 bit interface
[iii] Double Data Rate
[iv] Data Acquisitioner

The reference clock to the serializer is supplied externally, through the clock buffer CDCV304, from Lattice's clock generator **clk5620A**. This chip can generate 20 single ended or 10 pairs of differential clock signals with speeds up too 320 MHz. The evaluation board used in the thesis uses only 2 output pairs and thus 2 different differential, or 4 single ended clock signals is possible to generate. The evaluation board has an integrated 100 MHz oscillator which is used as reference clock, but it is also possible to connect an external clock as reference. Programming and setup is made by switches directly on the board and by use of the software PAC-designer, downloadable from Lattice's homepage[i].

As voltage supplies, in many of the designed circuit boards, the regulators in the **LT1763** series, are used. LT1763, produced by Linear, generates a low noise and stable output voltage. Input voltages to the regulators can vary a lot (a few volts up to 20 volts depending on model) and still generate the same output voltage. The series consists of two different types:

- The fixed output voltage type, supplying the voltages 2.5V, 3.3V, 5V etc. These models are named LT1763-2.5, LT1763-3.3 etc. where the last digits stand for the fixed output voltage.
- An adjustable output voltage model, simply named LT1763, capable of supplying 1.22-20 volts. The output voltage can be controlled by a connected potentiometer.

Two different packages are available and the package used in the thesis designs is "S8 PACKAGE 8-LEAD PLASTIC SO". Two of the models are used in the designed circuit boards – LT1763-2.5 and LT1763-3.3.

SMA (SubMiniature version A) connector is a coaxial RF[ii] connector with a minimal connector interface for coaxial cable with a screw type coupling mechanism. The connector has an impedance of 50 Ohm and offers excellent electrical performance from DC[iii] to 18 GHz. [27] SMA connectors are especially important for high speed electronics and are used on many of the designed circuit boards.

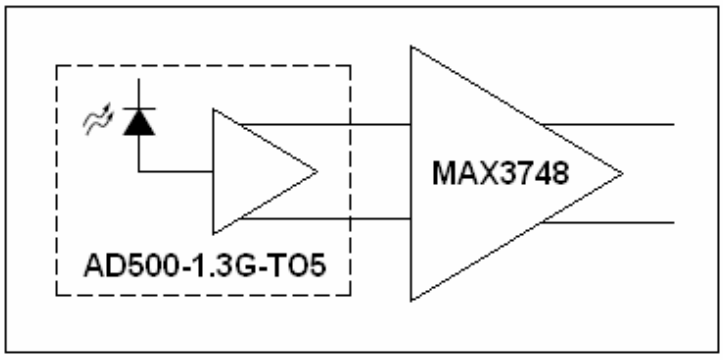

Figure 42: Designed high speed receiver circuit board.

[i] http://www.latticesemi.com/
[ii] Radio Frequency
[iii] Direct Current

The first step in the high speed receiver (seen in Figure 42) is Silicon Sensor's **AD500-1.3G-TO5**[i]. AD500 incorporates an internal TIA and APD, packaged in a hermetically sealed 5-pin TO-5 package. The APD has an active area diameter of 500 μm and can operate up to 1.3 GHz. To limit the current and thus prevent permanent failure of the device a large resistor should be placed in series with the APD.

As LA in the high speed receiver Maxim's **MAX3748** is used. This chip can operate over a wide bandwidth, down from 155 Mbit/s up to 4.25 Gbit/s. A wide range of input voltages is accepted and a constant voltage of 780 mV_{P-P}[ii] is provided at the output. The typical input and output impedance of the circuit is 50 Ω. The minimum input is ~5 mV_{P-P} and the maximum input is 1200 mV_{P-P}.

The VCSEL **PM67-F1P0N**[iii] is part of the high speed transmitter circuit board. This laser diode emits a 1.0 mW[iv] visible laser beam at 670 nm at a speed up to 2.5 Gbit/s [24]. With eye safety in mind, this laser is less dangerous compared to PH85 (used on the low speed receiver) due to the lower power and the visible light beam, but for precautions, protecting goggles is advisable.

[i] Called AD500 for short in the rest of the thesis
[ii] Typical value
[iii] PM67 for short in the rest of the thesis
[iv] At 4 mA and 25 ºC

4.1.4. High speed transmitter

The high speed transmitter is built around Linear's VCSEL driver LTC5100 and Optowell's VCSEL PM67-F1P0N. The VCSEL driver is supplied by a LT1763-3.3. The IN+ and IN- ports is internally AC coupled which makes external input capacitors unnecessary and minimizes circuit board size and component count. The schematic of the circuit board can be seen in Figure 43 and the top side layout can be seen in Figure 44. Top side of the finished circuit board can be seen in Figure 45. The top and bottom layer of the circuit board can also be seen in Appendix B.

To set and control parameters for the laser driver such as bias current, modulation current, fault configuration etc. an external memory, micro-processor or computer can be connected by I^2C[i] to the LTC5100 component. 128 bits is the smallest possible memory that can be used and then all of the memory spaces are used. The ports SDA[ii] and SCL[iii] should be pulled up to the supply voltage with external resistors but this is not needed when operated with this VCSEL driver because the circuit has an internal pull-up current sources for this purpose. In the thesis design 24LC00, a non-volatile 128 bits EEPROM, is used and connected to the circuit board. The EEPROM is easily connectable and removable by insertion into a soldered socket seen in Figure 46.

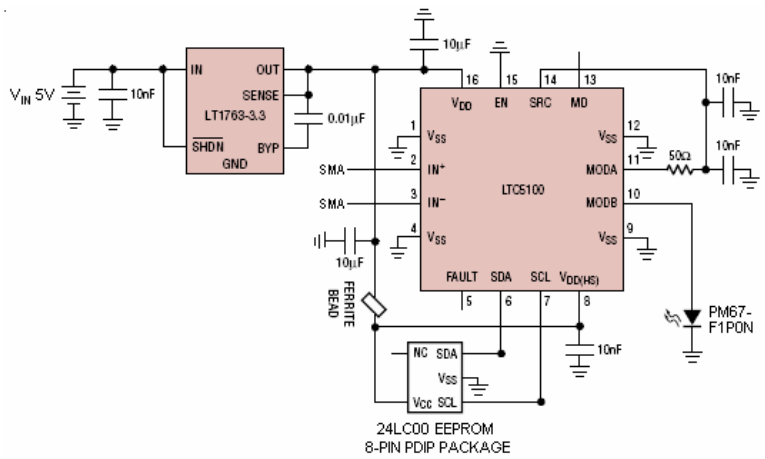

Figure 43: Design of the high speed transmitter. Be aware that the ferrite bead is removed and short circuited when soldering of the tested circuit board.

Below is an overall description of the circuit:

- The designed circuit board are based on the low reflection circuit described on page 48 in the VCSEL driver's datasheet [28].
- A copper circuit board is used with two layers (top and bottom). The bottom layer is used as ground plane and the top layer is floating.
- The ferrite bead is short circuited when soldering. This is because it should be possible to ad a ferrite bead if needed.

[i] I^2C stands for inter-integrated circuit and is a multi-master serial computer bus. It uses only two bidirectional lines, SDA and SCL.
[ii] Serial Data
[iii] Serial Clock

- Due to the difficulty of soldering small components by hand, 1206[i] size passive components are used instead of the 0402 size. 0402 is suggested in the datasheet [28].
- For easy connection and removability of the EEPROM, the bigger 8-PIN PDIP package is used instead of the datasheet suggested SOT23. The EEPROM is not soldered to the circuit board and thus makes it connectable and removable (for reprogramming) in a soldered socket.
- The IN+ and IN- pins with 50 Ω in input impedance are connected with SMA connectors (also 50 Ω).
- Due to the small circuit size and difficulty of soldering vias by hand, no vias are connected to the exposed pad. At least 4 vias is suggested in the datasheet.
- Each via hole has a diameter of 0.6 mm and each via pad a diameter of 1.2 mm on each side (front- and backside).
- To connect the front- and backside of the vias, a short trace is soldered through the board.
- For simplicity the enable pin is connected directly to ground. This means that the laser cannot be turned on or off by hand. This also means that the enable pin polarity in the VCSEL driver setup must be set to “active low” (en_polarity = 0).
- Instead of the datasheet solution with the laser connected via a 50 Ohm coaxial cable the VCSEL is connected directly to the circuit board.
- To minimize the number of vias used the EEPROM is connected to the backside of the circuit board. This also makes placement of the laser close to the detector easier.
- The SMA connectors are connected on the circuit board backside to spare the use of vias at the IN+ and IN- traces.
- The ground and LT1763-3.3 supply is soldered to the red wires seen in Figure 45.
- The 4 mm holes placed in the corners makes it possible to attach the circuit board to a measurement set-up for proper alignment to a receiver when testing.
- The output of the laser driver is not perfectly matched with the VCSEL. A 50 Ohm resistor is connected between SRC and MODA. To optimize matching the series resistance[ii] of the PM67 should be used instead.

[i] 1.2 mm length and 0.6 mm width
[ii] 50 Ohm typical value, 90 Ohm maximum value (25 C, I = 4 mA)

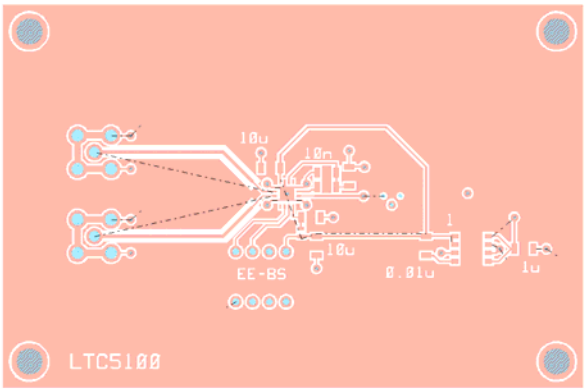

Figure 44: Top layer layout of the LTC5100 laser driver circuit board.

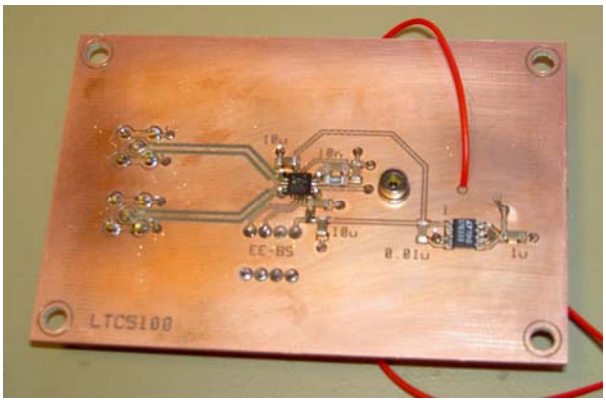

Figure 45: Top layer of the produced LTC5100 laser driver circuit board in the project.

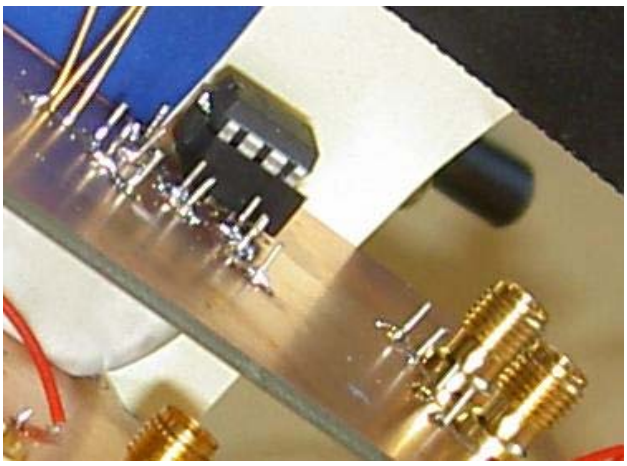

Figure 46: The 24LC00 EEPROM attached to a socket on the "bottom side" of the LTC5100 circuit board.

4.1.4.1. Setup of the VCSEL driver's parameters

Most of the VCSEL driver's parameters can be obtained with the use of the LTC5100 evaluation software in simulation mode. The software (Figure 48) can be downloaded from Linear's homepage[i]. In the software the following parameters are set:

- Constant current control (CCC) mode is set (Apc_en = 0). In this mode the laser current is controlled directly with no feedback from a monitoring photodiode. The laser current can be temperature compensated, but this is not used in the thesis design.
- CML_en set to 1. Current mode logic (CML) set so 50 Ohm termination to ground is used at the two input terminals (IN+ and IN-). The other possible option is 100 Ohm termination between the two input terminals. The 50 Ohm configuration is used because it gives a higher possible maximum input voltage at the input terminals which is suitable when clk5620 is used as input signal to the LTC5100.
- Standalone operation is set (Operating_mode set to 0). In this mode parameters are loaded from an external EEPROM instead from an external microprocessor or computer.

[i] http://www.linear.com

- The bias current (I_B in Figure 47) is set to 4 mA (Ib_nom set to 455).
- The modulation current (I_M in Figure 47) is set to 2 mA (Im_nom set to 227). Observe that the exact actual modulation current running through the laser diode depends on the termination resistor (R_T) and the dynamic resistance of the laser diode (R_{LD}) shown in Figure 47. The actual current can be calculated by the formulas (1), (2) and (3) on page 17 in the datasheet [28].
- Transmitter enabled (Soft_en = 1).
- All other parameters are set to the default values obtained from the LTC5100 evaluation software, and all of the parameters selected are shown in Appendix B. The creation of the hexagonal programming code can be followed step by step in appendix B. The hexagonal code is created because the EEPROM programmer software requires hexagonal numbers.

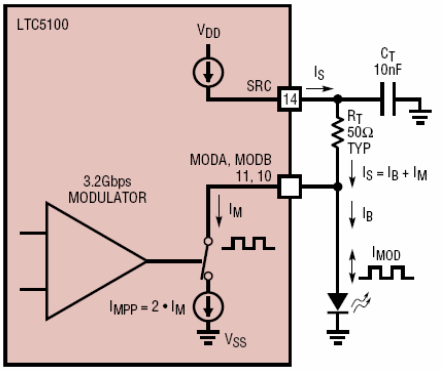

Figure 47: Simplified model of the laser bias and modulation circuit. [28]

To setup the EEPROM the device programmer **PIKprog2** can be used. This programmer is able to program several different types of microchips and is connectable to a computer via a USB connector. The program PG4UW, downloadable from ELNEC's homepage[i], is used to program the microchip.

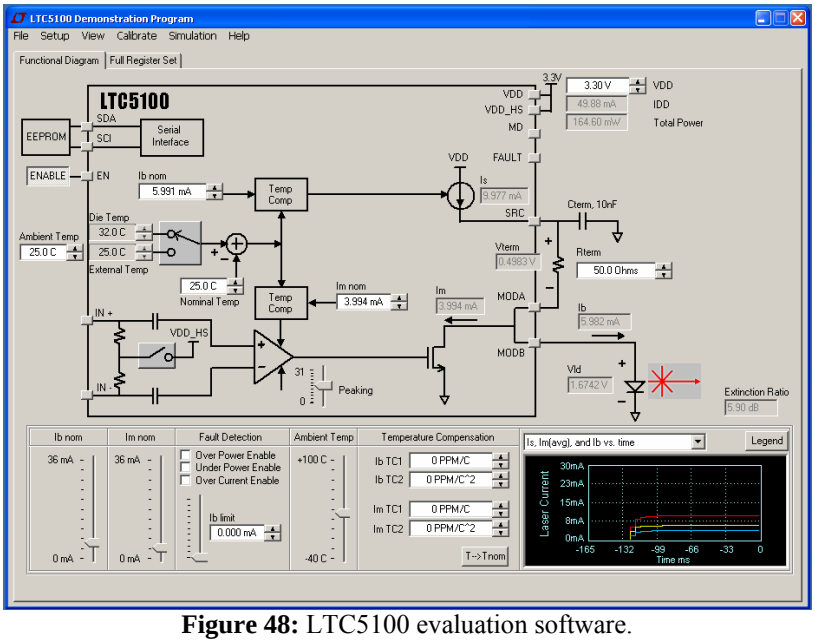

Figure 48: LTC5100 evaluation software.

[i] http://www.elnec.com/

4.1.5. High speed receiver

The designed high speed receiver is composed of an avalanche photodiode, a transimpedance amplifier and a limiting amp; all components are connected to the same circuit board. The APD and TIA is part of the single chip AD500-1.3G-TO5 produced by Silicon sensor, and the LA (MAX3748) is produced by Maxim. The top and bottom layer layout can be seen in Figure 50 and Appendix A. The design (seen in Figure 49) of the receiver circuit board is described below:

- A copper circuit board is used with two layers (top and bottom). The bottom layer is used as ground plane and the top layer is floating. All components (except the AD500) and all traces are placed on the top layer.
- The AD500 is connected with top side on the circuit board's backside.
- Each via hole has a diameter of 0.6 mm and each via pad a diameter of 1.2 mm on each side (front- and backside).
- To connect the front- and backside of the vias, a short trace is soldered through each via.
- To test the APD/TIA and LA individually SMA1, SMA2, R_{TIA+}, R_{TIA-}, $R_{SMA\ IN+}$, $R_{SMA\ IN-}$, $R_{SMA\ GND+}$ and $R_{SMA\ GND-}$ are connected to the board. The selection of size of these resistors is described in section 4.2.1.1. For the circuit board to function as an APD/TIA/LA receiver the resistors R_{TIA+} and R_{TIA-} should be short circuited.
- The resistors $R_{SMA\ IN+}$ and $R_{SMA\ IN-}$ are set to 680 Ω and $R_{SMA\ GND+}$ and $R_{SMA\ GND-}$ are set to 50 Ω. This configuration is used to be able to test the LA individually with a external signal as simulated TIA. The input impedance is calculated in formula (4:1).
- All SMA connectors are connected on the circuit board's backside to avoid the use of vias for the signal traces.
- For noise reduction a 0.001 µF capacitor is connected close to each of the four V_{CC} pins on the MAX3748.
- AC coupling setup by connection of 0.1 µF capacitors at the input and output of the MAX3748.
- The TIA's 5V supply is filtered with a 10 µF and a 0.1 µF capacitor.
- To protect the circuit and APD against high currents, a 390 kΩ resistor is connected as suggested in the datasheet.
- The LOS function (described in the datasheet) is disabled by connection of the TH pin to 3.3 V. This reduces power consumption.
- Between CAZ1 and CAZ2 a capacitor of 0.1 µF (typical value) is connected. The function of these pins is described in the datasheet.
- The 4 mm holes placed in the corners makes it possible to attach the circuit board to a measurement set-up for proper alignment to a receiver when testing.

Because, $R_{SMA\ IN+} = R_{SMA\ IN-} = R_{SMA\ IN}$ is big (680Ω) compared to $R_{SMA\ GND+} = R_{SMA\ GND-} = R_{SMA\ GND}$ (50Ω), the input impedance seen from the SMA connectors (Z_{input}) can be approximated as

$$Z_{input} = \left(R_{SMA\ IN} + Z_{IN}\right) \| R_{SMA\ GND} \approx R_{SMA\ GND} = 50\Omega\,, \qquad (4:1)$$

where $Z_{IN+} = Z_{IN-} = Z_{IN}$ is the input impedance of the MAX3748. In the above formula C_{IN-} and C_{IN+} is seen as short circuited and are for that reason not present.

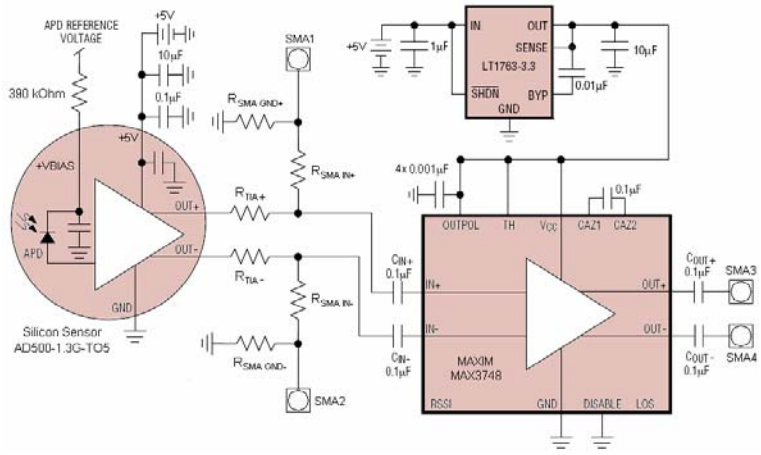

Figure 49: Schematic of the high speed receiver circuit board.

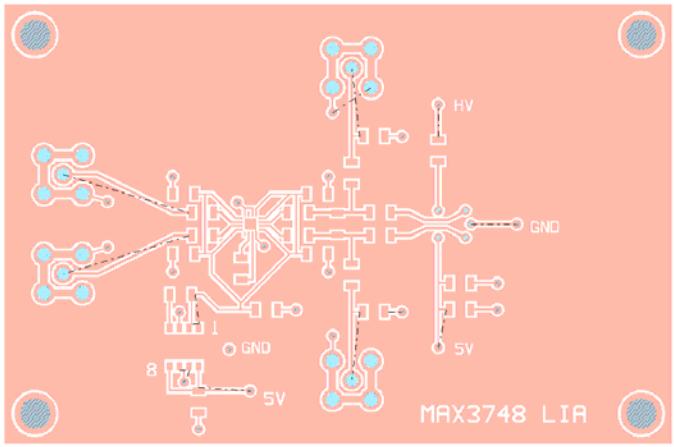

Figure 50: Top layer layout of the high speed receiver AD500-1.3G-TO5/MAX3748.

4.1.6. Serializer circuit board

To be able to feed data fast enough to the laser driver (LTC5100) the serializer circuit board, seen in Figure 52, is needed. The 10 bit serializer circuit used is the model TLK1201AI. This component is able to send (and receive) data at speeds from 600 Mbit/s to 1.3 Gbit/s. The multiple signals at the inputs of the serializer is multiplexed and then transmitted (to the laser driver) at the differential output (as seen in Figure 54). Normally a serializer is used in this stage (before the laser driver). Because the input ports (TD0-TD9 in Figure 53) in this design are connected by non-shielded wires, the circuit is only built to handle low speed signals at these ports. Because the serializer circuit board is just a test circuit, the 10 inputs are connected to constant voltages when tested. By keeping the input bits of the serializer constant other components or testing equipment in front of the SERDES sending data, can be eliminated and thus only a constant voltage generator (Digital controller in Figure 53) is required. The digital out of the DAQ (U2356A) is used in the tests (in section 4.2) as the digital controller. The schematic can be seen in Figure 53. The top and bottom layout can be seen in Appendix A and Figure 51. Below is a short description of the constructed circuit board:

- Only the transmitting part (serializer) of the SERDES is used.
- A Texas instruments clock buffer (CDCV304) is soldered to the circuit board at the reference clock input (REFCLK) to minimize noise. One output (three available) of the clock buffer is used.
- The CDCV304 is supplied by a LT1763-3.3.
- The TLK1201AI is supplied by a LT1763-2.5.
- The differential output and clock input is connected by SMA.
- The ferrite bead connected is the model BLM18EG121SN1 (120 Ω at 100 MHz and 145 Ω at 1 GHz).
- The inputs, TD0-TD9 and MODESEL, are connected by soldered wires as seen in Figure 52.

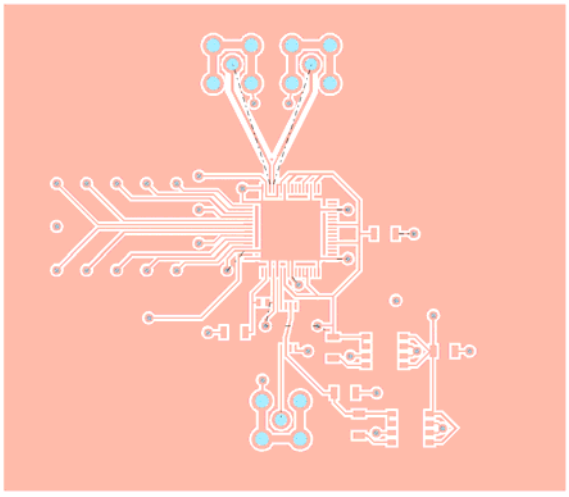

Figure 51: Top side layout of the serializer circuit board.

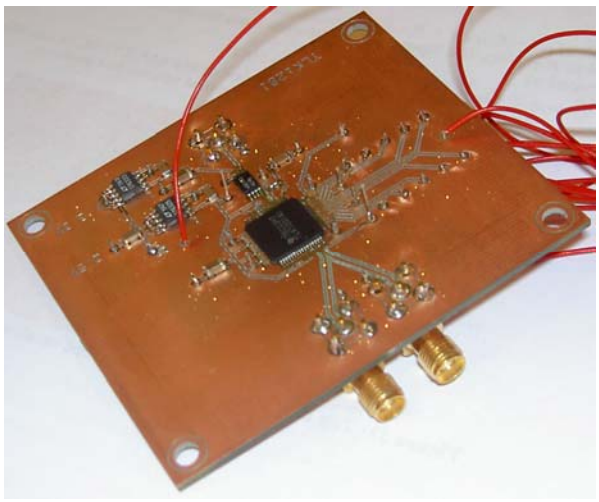

Figure 52: The serializer circuit board.

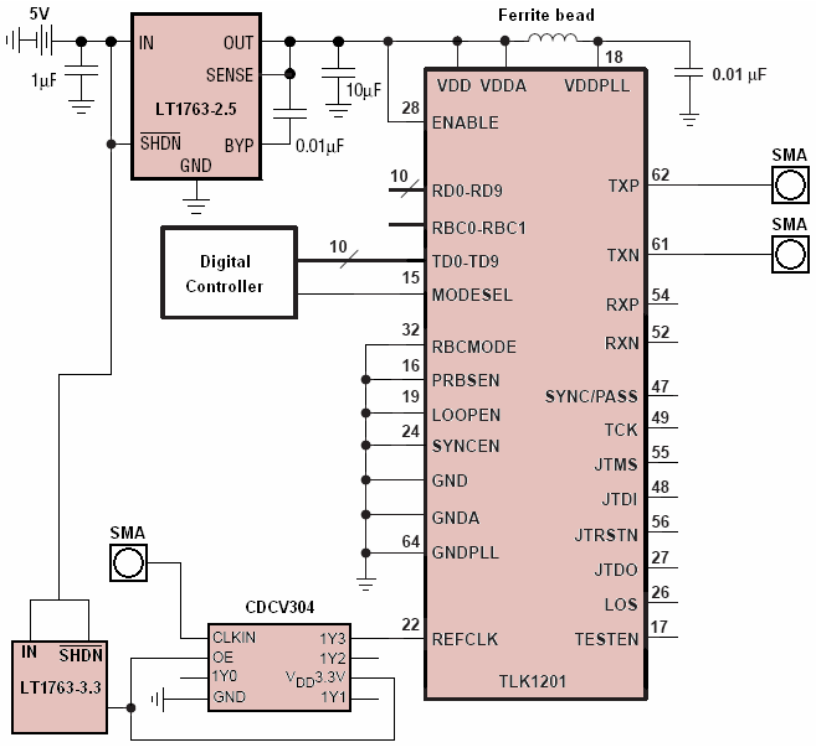

Figure 53: The schematic of the serializer circuit board. The LT1763-3.3 is configured the same way at OUT, SENSE and BYP (with capacitors) as the LT1763-2.5.

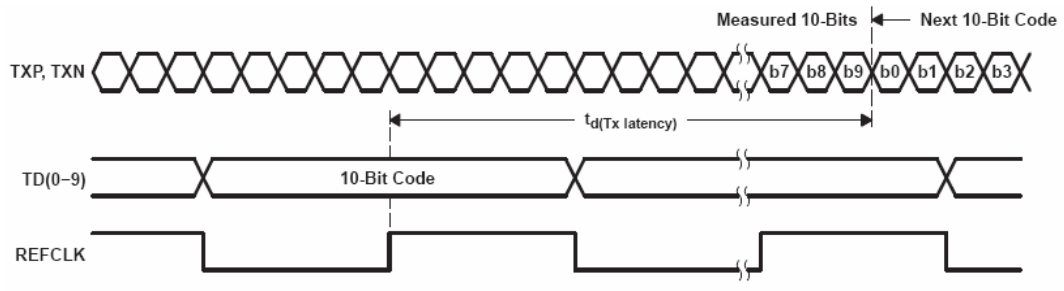

Figure 54: TLK1201AI in TBI mode. [29]

4.2. Test results

4.2.1. Low speed oscilloscope tests

In this chapter the tests with a low speed oscilloscope are described. These initial tests are performed because no high speed oscilloscope was available at the time of testing, and are supposed to provide preliminary design feedback.

4.2.1.1. High speed receiver

4.2.1.1.1. Limiting amplifier with simulated TIA signal

To test the limiting amp on the high speed receiver circuit board, an input signal from the TIA is simulated with Lattice's clock generator clk5620. Because the maximum signal from a TIA is small (up to a few hundred mV_{P-P} for AD500-1.3G-TO5) and the minimum overload signal at the input of the MAX3748 is only 1200 mV_{P-P}, the output signal of the clk5620 has to be voltage divided. The voltage divide circuit can be seen in Figure 55 and the signal obtained at the input is calculated using equation (4:3) and (4:4). The test setup can be seen in Figure 56 and a measured signal can be seen in Figure 57.

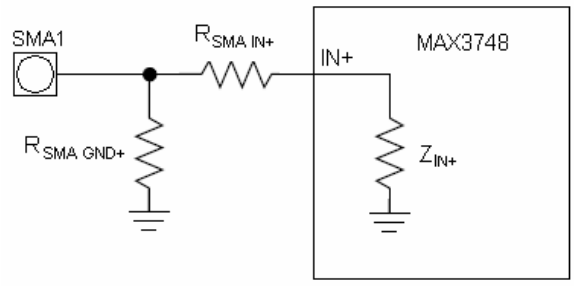

Figure 55: The OCOM receiver's SMA1 input stage when the resistor R_{TIA+} not connected and C_{IN+} short circuited.

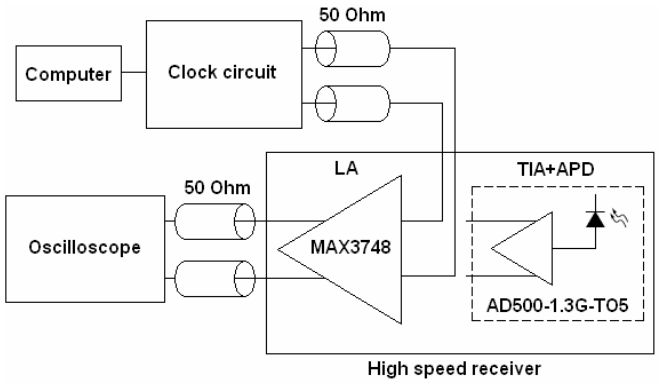

Figure 56: Setup of the MAX3748 test.

The simplified input stage at SMA1 when ignoring C_{IN+} and removing R_{TIA+}, can be seen in Figure 55. When setting $R_{SMA\ IN+}$ to 680 Ω, $R_{SMA\ GND+}$ to 50 Ω, the signal at the input of the MAX3748 (V_{LA+}) can be calculated in terms of V_{IN+} (signal at SMA1). Because the same resistors are used on the SMA2 side, V_{LA} = V_{LA+} = V_{LA-} can be calculated in terms of V_{IN} = V_{IN+} = V_{IN-} as

$$V_{LA} = V_{LA+} = V_{LA-} \approx \frac{1}{1 + \frac{R_{SMA\ IN}}{Z_{IN}}} V_{IN} = \frac{1}{1 + \frac{680}{50}} V_{IN} \approx 0.07 V_{IN}. \quad (4:2)$$

Z_{IN} is the input impedance of MAX3748 (50 Ω).

By using (4:2) and an input signal (V_{IN}) of 3.3 volts the voltage at the LA's input voltage (V_{LA}) is

$$V_{LA} \approx 0.07 V_{IN} = 230 \text{ mV}. \quad (4:3)$$

If the signal at SMA1 and SMA2 is differential the differential input signal ($V_{LA\text{-}Differential}$) at the LA is calculated as

$$V_{LA-differential} = 2 \cdot V_{LA} \approx 0.14 V_{IN} = 460 \text{ mV}. \quad (4:4)$$

The test is set up in the following way:

- The clock generator clk5620 set to 3.3V LVTTL, is used as a differential input signal at SMA1 and SMA2 (one of the ports was inverted). This gives the differential input signal at the LA as calculated above ($V_{LA\text{-}differential}$).
- The signal from the clock generator is set to 60 MHz.
- R_{TIA+} and R_{TIA-} were removed (i.e. set to infinity).
- The output signal from the limiting amp (MAX3748) is measured with an oscilloscope (Tektronix TDS 210) with a bandwidth of 60 MHz and a sample rate of 1 Gs/s (Giga sample per second). The test result was transferred from the oscilloscope to a connected computer.
- To match the input and output impedance, 50 Ω coaxial cables are used to connect the oscilloscope and clock generator.
- To be able to measure a differential output signal from the limiting amp the signal on one channel (OUT-) is inverted and the both signals are added by the MATH function (CH1 + CH2) on the oscilloscope.

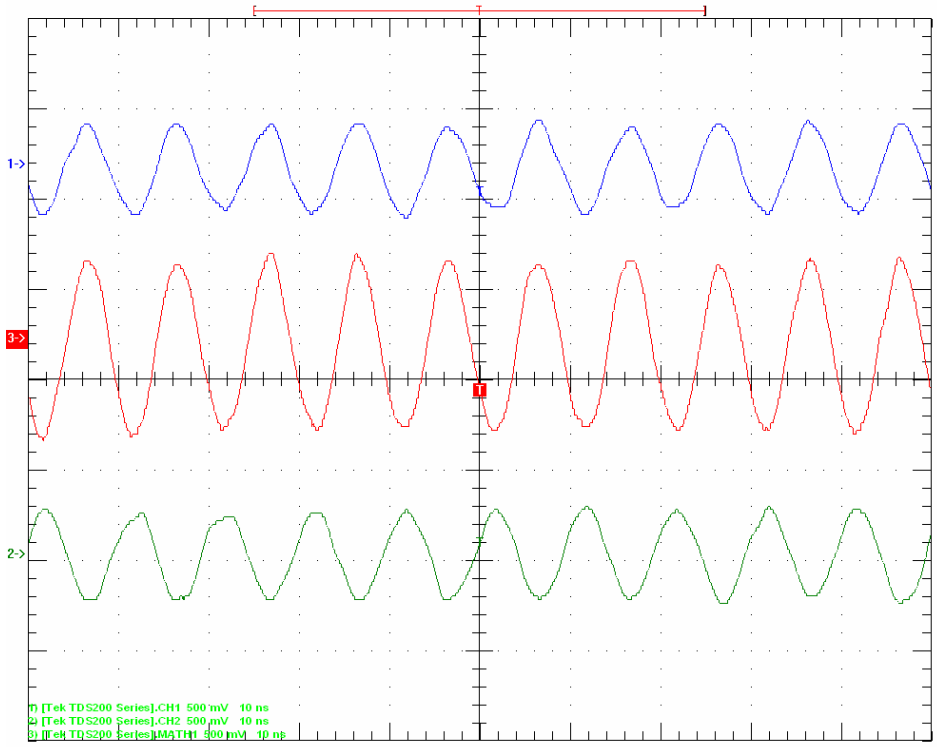

Figure 57: Signal measured from the MAX3748 with 100 MHz input signal from clk5620. The top and bottom signal is measured single ended. The middle signal is obtained by the CH1+CH2 (after inverting one signal on the oscilloscope) function on the oscilloscope. The voltage and time step length are 500 mV and 10 ns. The signal is not averaged by the oscilloscope.

4.2.1.2. High speed transmitter and receiver

In this test the high speed transmitter is tested with the receiver circuit board. Two tests are made with little difference in alignment between the VCSEL and the photodiode. The output signal is measured with a 60 MHz bandwidth oscilloscope. The test setup can be seen in Figure 58.

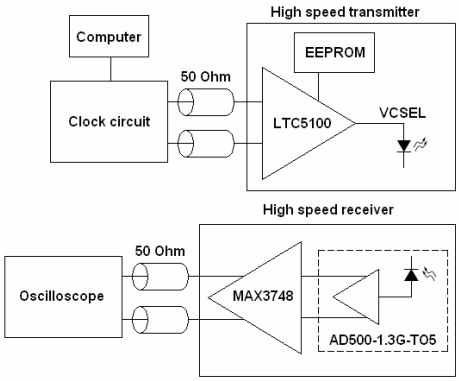

Figure 58: Setup of the transmitter to receiver test.

The results of the measured signal from the limiting amp can be seen in Figure 60 and Figure 61, and the test parameters are as follows:

- The EEPROM parameter code used is described in section 4.1.4.1.
- The output signal from the limiting amp (MAX3748) was measured with an oscilloscope (Tektronix TDS 210) with a bandwidth of 60 MHz and the sample rate 1 Gs/s (Giga sample per second). The test result was transferred from the oscilloscope to a connected computer.
- As differential input signal to the laser driver LTC5100 (IN+ and IN-), the clock generator clk5620 was used. The signal from the clock generator was set to 60 MHz, 3.3 V and LVTTL (Low Voltage Transistor Transistor Logic). One of the ports was inverted to create a differential signal.
- To match the input and output impedance the signal cables used are 50 Ω coaxial cables.
- The transmitter and receiver is placed in close vicinity (~1 cm) and points towards each other. The physical setup can be seen in Figure 59.
- The differential output signal from the limiting amp is constructed by inverting the signal on one channel (OUT-) and adding the both signals by the MATH function (CH1 + CH2) on the oscilloscope.

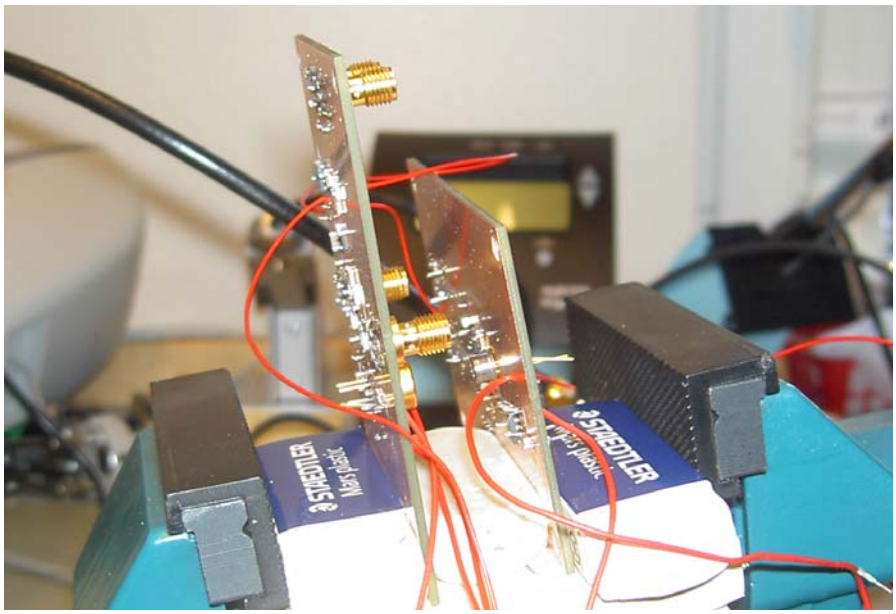

Figure 59: The physical setup and alignment of the transmitter and receiver. The transmitter is to the right and the receiver to the left.

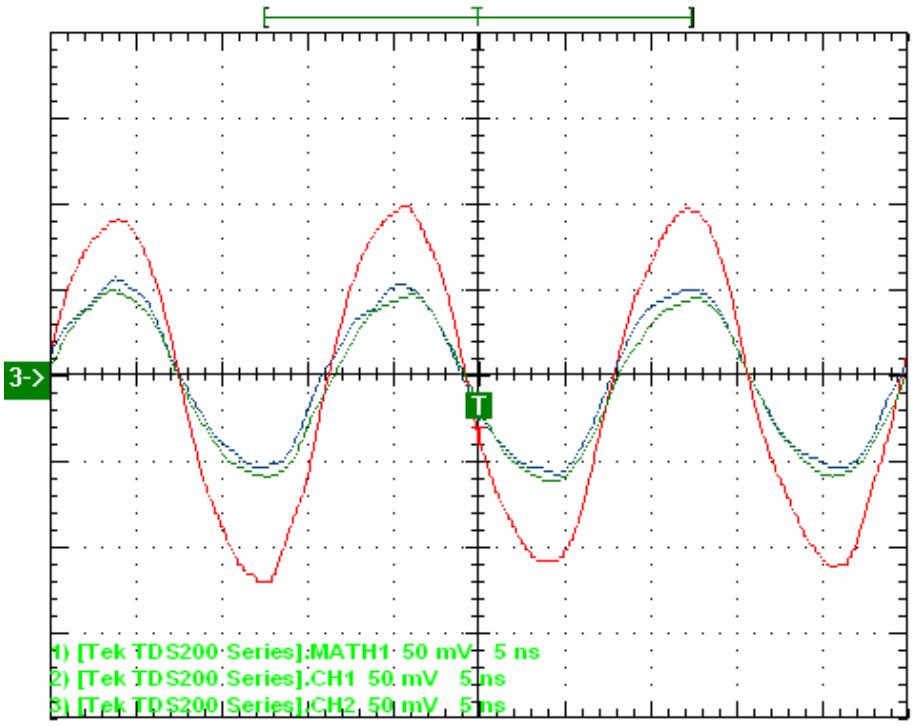

Figure 60: The signals measured at the MAX3748 limiting amp output when illuminated by the high speed transmitter in 60 MHz. The blue signal is measured at OUT+, the green signal is measured at OUT- (but inverted in the oscilloscope) and the red signal is obtained by adding OUT+ and OUT- (inverted) in the oscilloscope. The time step is 5 ns and the voltage step is 50 mV. The signal is not averaged by the oscilloscope.

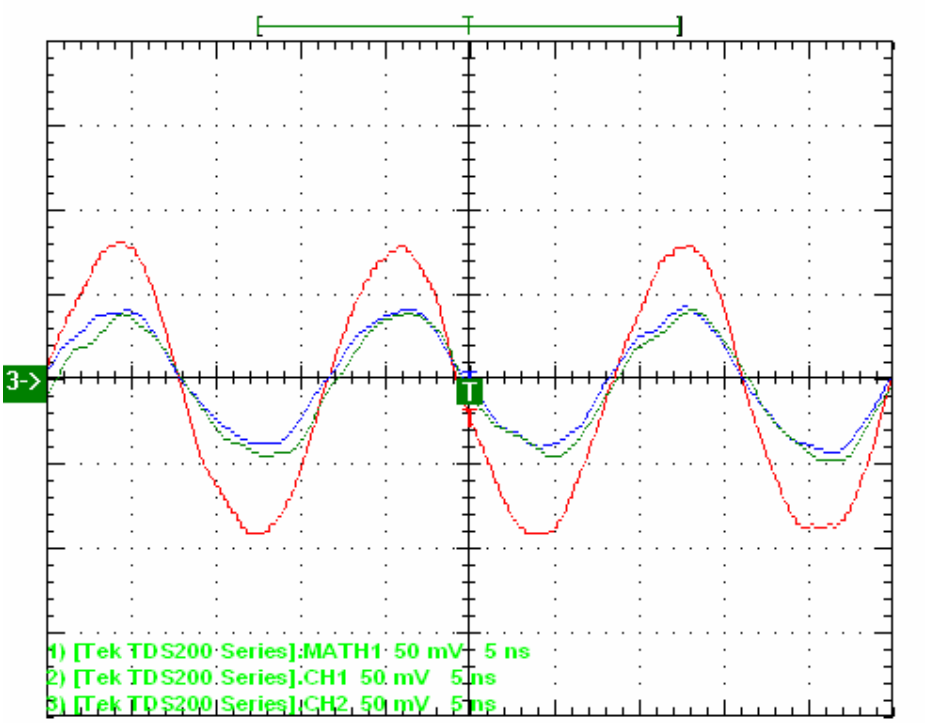

Figure 61: The signals measured at the MAX3748 limiting amp output when illuminated by the high speed transmitter in 60 MHz. The blue signal is measured at OUT+, the green signal is measured at OUT- (but inverted in the oscilloscope) and the red signal is obtained by adding OUT+ and OUT- (inverted) in the oscilloscope. The time step is 5 ns and the voltage step is 50 mV. The signal is not averaged by the oscilloscope.

4.2.1.3. Serializer circuit board

A test of the serializer circuit board in TBI mode is performed by feeding the serializer with a clock signal (clk5620) and alternating the 10 bit input with the DAQ (U2356A). The output signal is measured with the oscilloscope Tektronix TDS 210 (section 4.2.1.2). The results can be seen in Figure 63 to Figure 66.

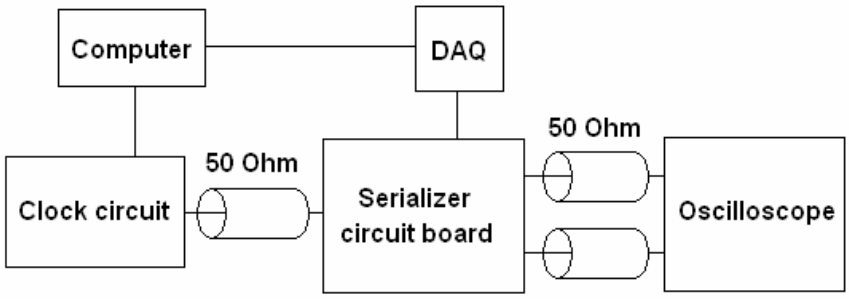

Figure 62: Setup of the serializer test.

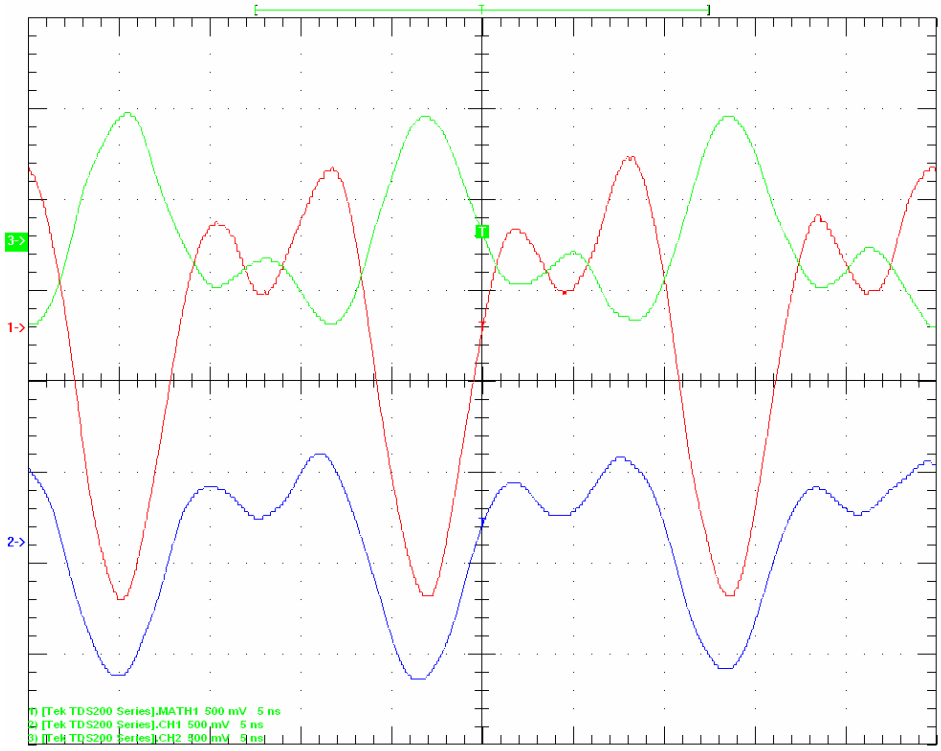

Figure 63: Signal measured from the serializer with the input signal 1110001110. The blue (TXP) and green (TXN) signal is measured single ended. The red signal is obtained by the CH1+CH2 (after inverting one signal on the oscilloscope) function on the oscilloscope. Voltage and time step length of 500 mV and 5 ns. The frequency of the clock signal is 60 MHz. This signal is not averaged by the oscilloscope.

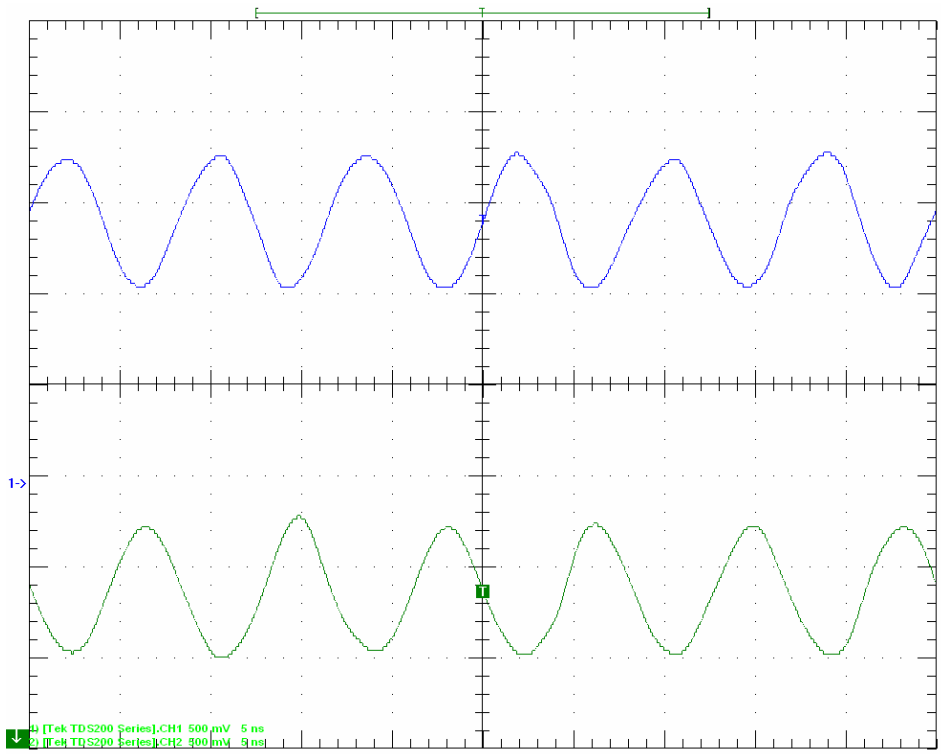

Figure 64: Signal measured from the serializer with the input signal 1110011100. The blue (TXP) and green (TXN) signal is measured single ended. Voltage and time step length of 500 mV and 5 ns. The frequency of the clock signal is 60 MHz. This signal is not averaged by the oscilloscope.

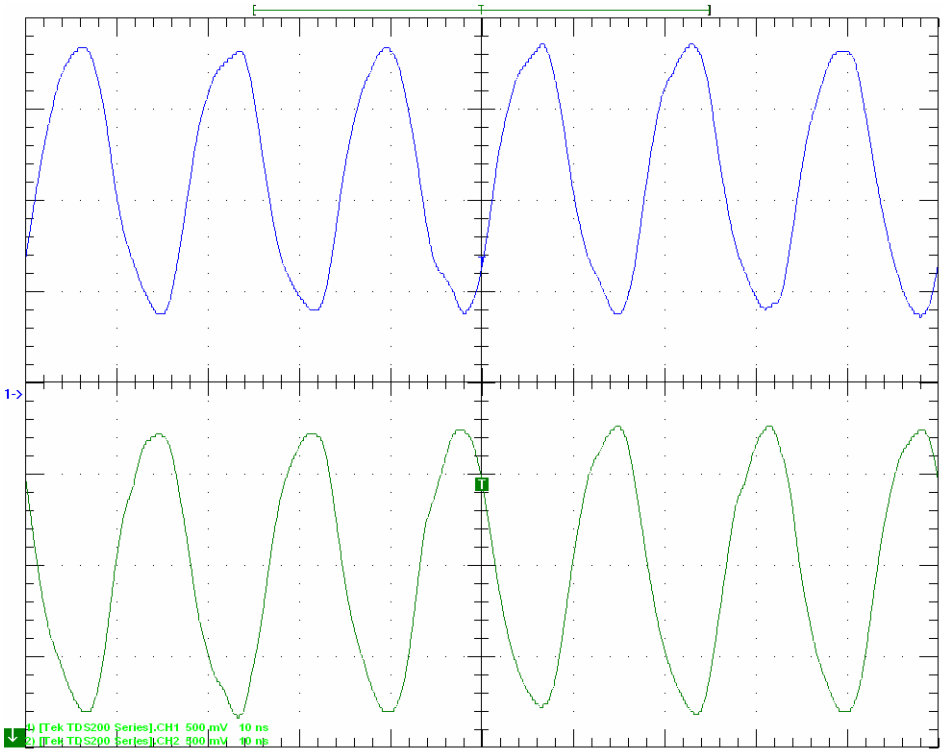

Figure 65: Signal measured from the serializer with the input signal 1110011100. The blue (TXP) and green (TXN) signal is measured single ended. Voltage and time step length are 500 mV and 10 ns. The frequency of the clock signal is 60 MHz. This signal is not averaged by the oscilloscope.

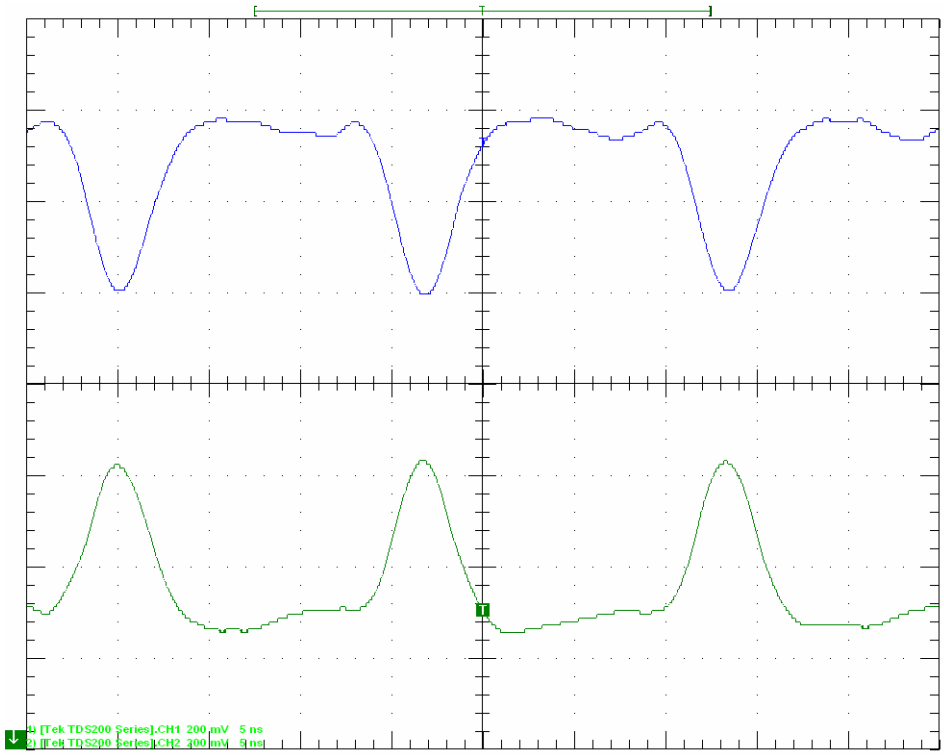

Figure 66: Signal measured from the serializer with the input signal 1111111110. The blue (TXP) and green (TXN) signal is measured single ended. Voltage and time step length are 200 mV and 5 ns. The frequency of the clock signal is 60 MHz. This signal is not averaged by the oscilloscope.

4.2.2. High speed oscilloscope tests

The overview of the tests performed with a high speed oscilloscope:

- Measure the clock signal.
- Measurement of the output signal from the serializer circuit board with different inputs (from the DAQ). Different speeds will be tested by altering the output from the clock circuit.
- Measure the output from the high speed receiver, when illuminated by the high speed transmitter with a signal supplied by the serializer. This is the main test. When this test is performed, use of laser protecting goggles is advisable.
- The oscilloscope used is Agilent's Infinium DCS 86100B. This is a wide bandwidth oscilloscope (65 GHz).
- A supply of 130 volts is connected to the APD (AD500).
- A computer is used to control the DAQ (U2356A) and clock circuit (clk5620A).
- The clock signal is used as trigger to the oscilloscope.
- Because the high speed oscilloscope (Agilent's Infinium DCS 86100B) does not have differential input, all measurements in section 4.2.2 are made single ended. In order to obtain a good result during single ended measurements; the second output port is terminated by a 50 Ω load. A serializer measurement with no termination used at the open port can be seen in Figure 74.
- The serializer is set too TBI mode.
- The clock circuit is set to LVTTL 3.3 volts.

4.2.2.1. Clock signal

Measurement of the clock signal (clk5620A) set to 80 MHz. The measured signal is shown in Figure 68 and the setup is shown in Figure 67.

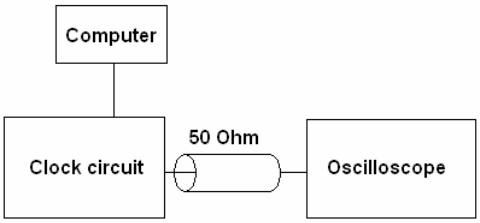

Figure 67: Clock measurement.

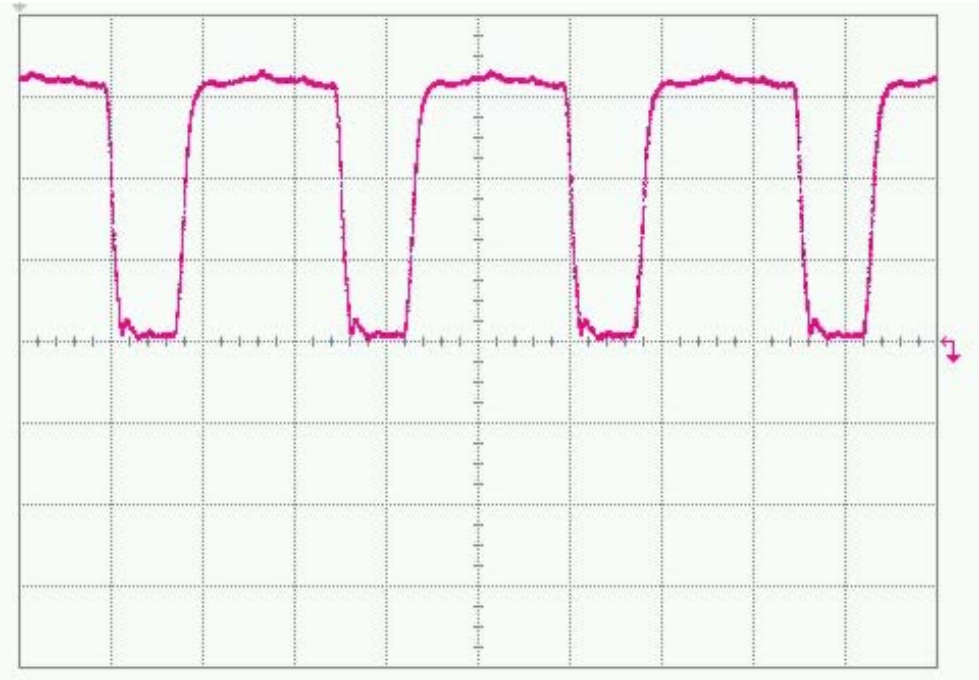

Figure 68: Measurement of the clk5620 at 80 MHz. Voltage and time step length of 500 mV and 5 ns. The small arrow to the right is the ground level.

4.2.2.2. Serializer

The clock circuit is used as trigger to the oscilloscope. To reach 1 Gbit/s the speed of the clock circuit is set to 100 MHz. A test of the maximum speed is also performed 1.3 Gbit/s (130 MHz clock signal). Different input to the serializer is tested by control of the DAQ. The measurement results are shown in Figure 70 to Figure 74.

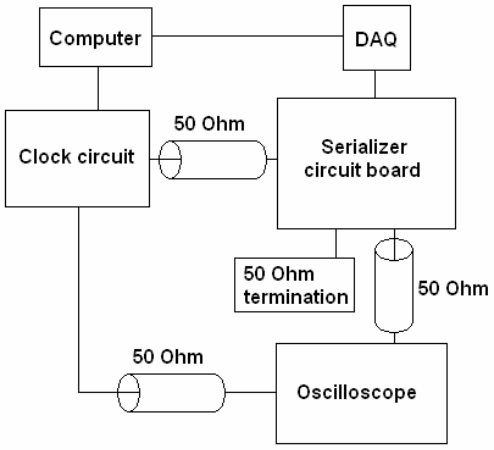

Figure 69: Serializer test.

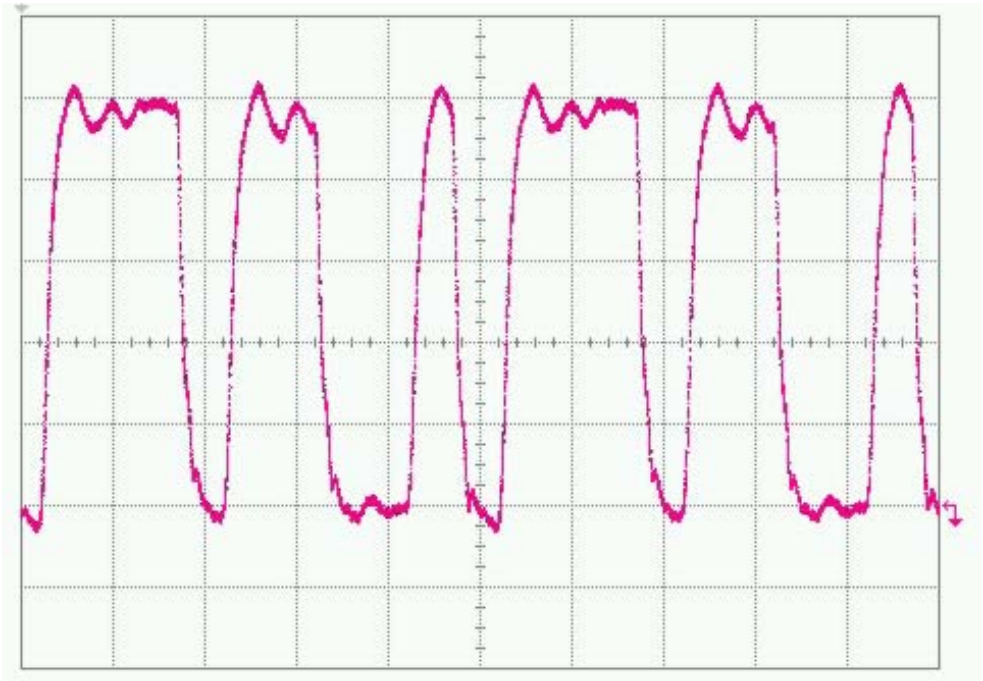

Figure 70: Single ended output (TXP) measurement of the serializer circuit board. The input clock is 100 MHz. TX0-TX9 1010011011 Obs. Voltage and time step length of 200 mV and 2 ns. The small arrow to the right is the ground level.

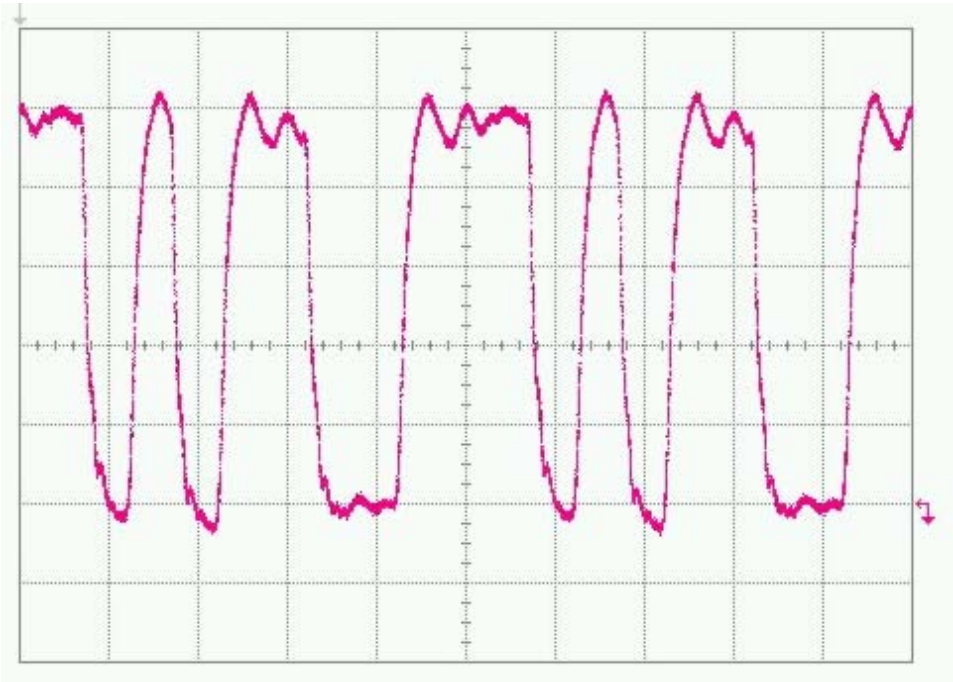

Figure 71: Single ended (TXP) output measurement of the serializer circuit board. The input clock is 100 MHz. TX0-TX9 1110011010 Obs. Voltage and time step length of 200 mV and 2 ns. The small arrow to the right is the ground level.

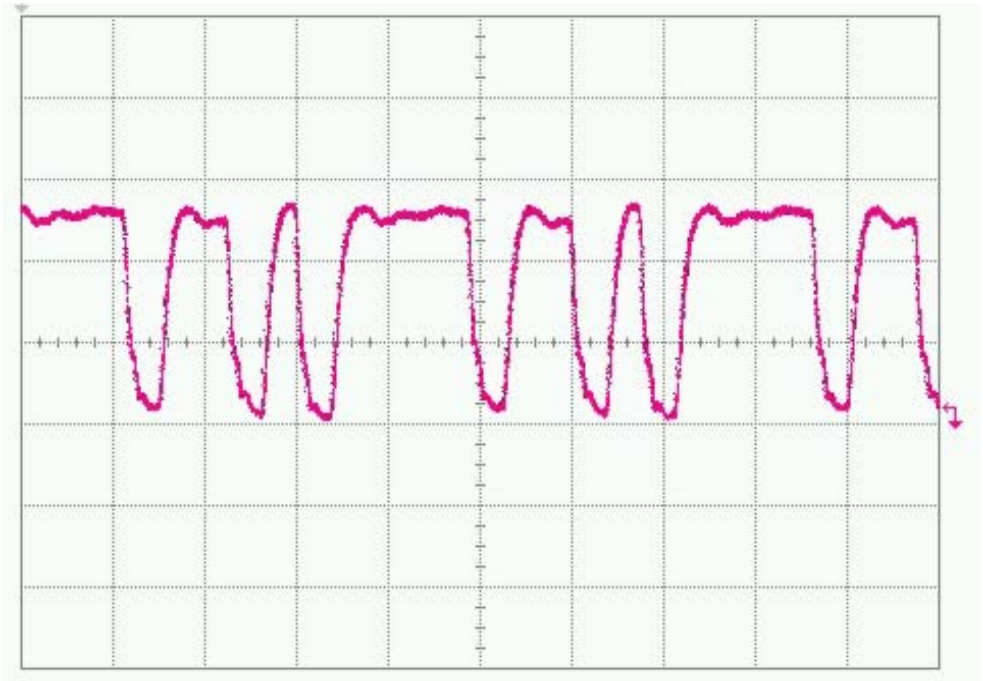

Figure 72: Single ended (TXP) output measurement of the serializer circuit board. The input clock is 130 MHz. TX0-TX9 set to 1011011110 Obs. Voltage and time step length of 500 mV and 2 ns. The small arrow to the right is the ground level.

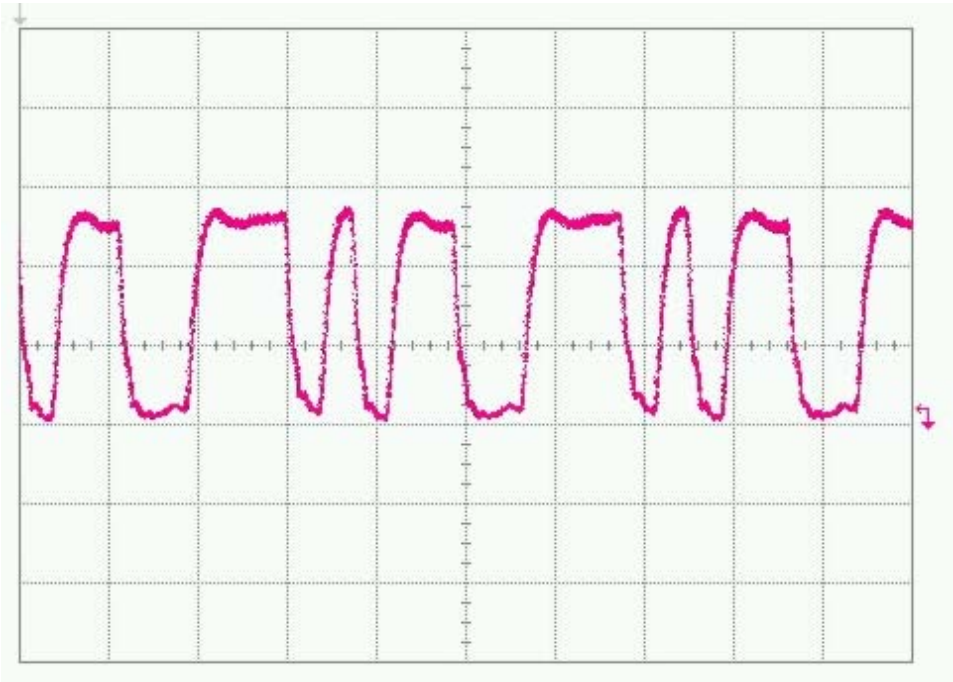

Figure 73: Single ended output (TXP) measurement of the serializer circuit board. The input clock is 130 MHz. TX0-TX9 set to 1110011010 Obs. Voltage and time step length of 500 mV and 2 ns. The small arrow to the right is the ground level.

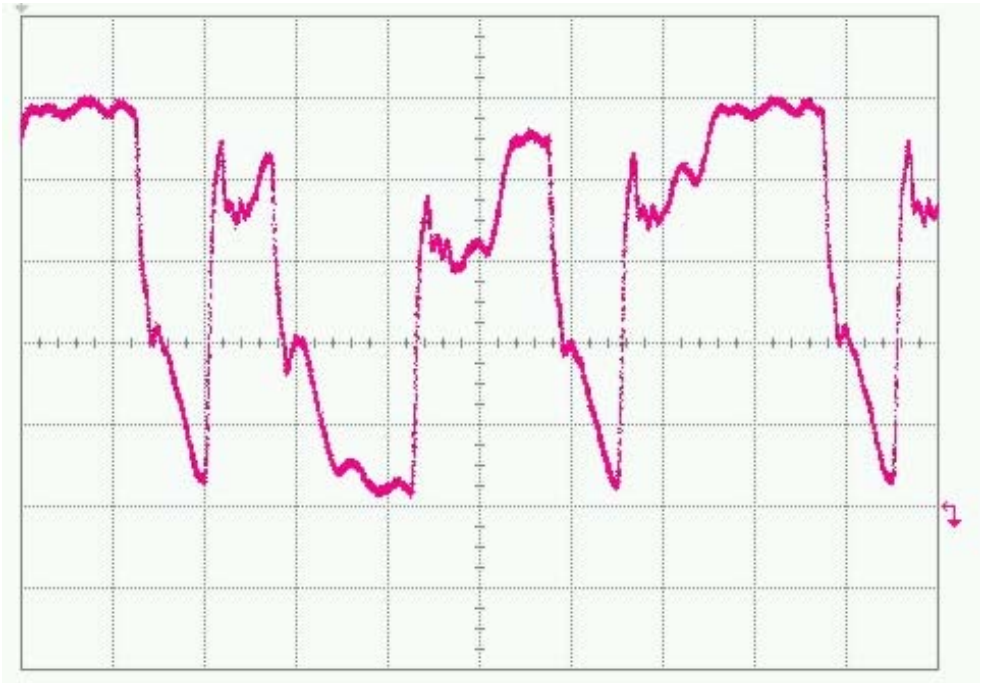

Figure 74: Single ended (TXP) output measurement of the serializer circuit board. The input clock is 130 MHz. 66.7 MHz. TXN is not terminated by 50 Ω. Voltage and time step length of 200 mV and 2 ns. The small arrow to the right is the ground level.

4.2.2.3. Optical link – Serializer, high speed transmitter and receiver

In order to test the serializer, transmitter and receiver the following test is setup. Different input to the serializer is tested by control of the DAQ. Single ended measurement by the oscilloscope. The measurement results are shown in Figure 77 to Figure 82. The VCSEL and APD are placed in close vicinity (~0.5 cm) and points towards each other. Setup and physical setup can be seen in Figure 75 and Figure 76. The EEPROM parameter code used is described in section 4.1.4.1 and Appendix B.

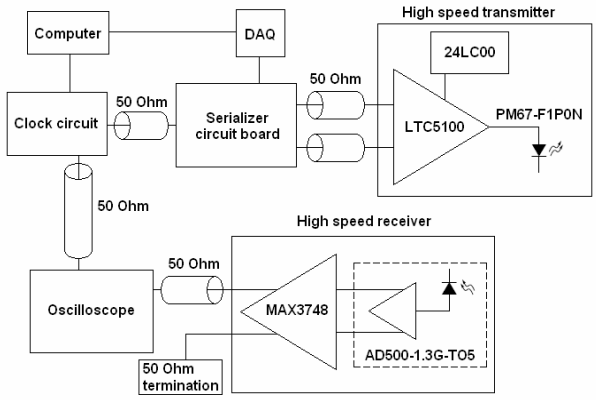

Figure 75: Serializer to limiting amp test.

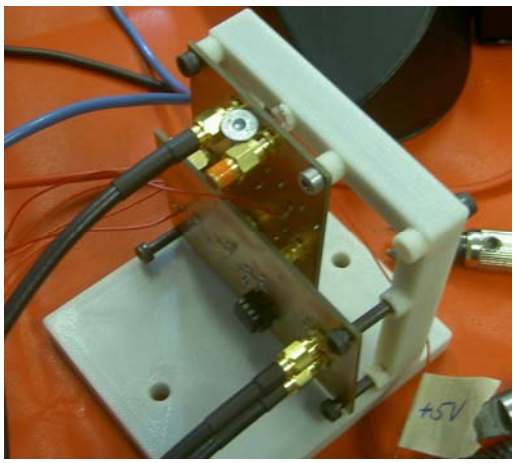

Figure 76: Physical setup in fixture.

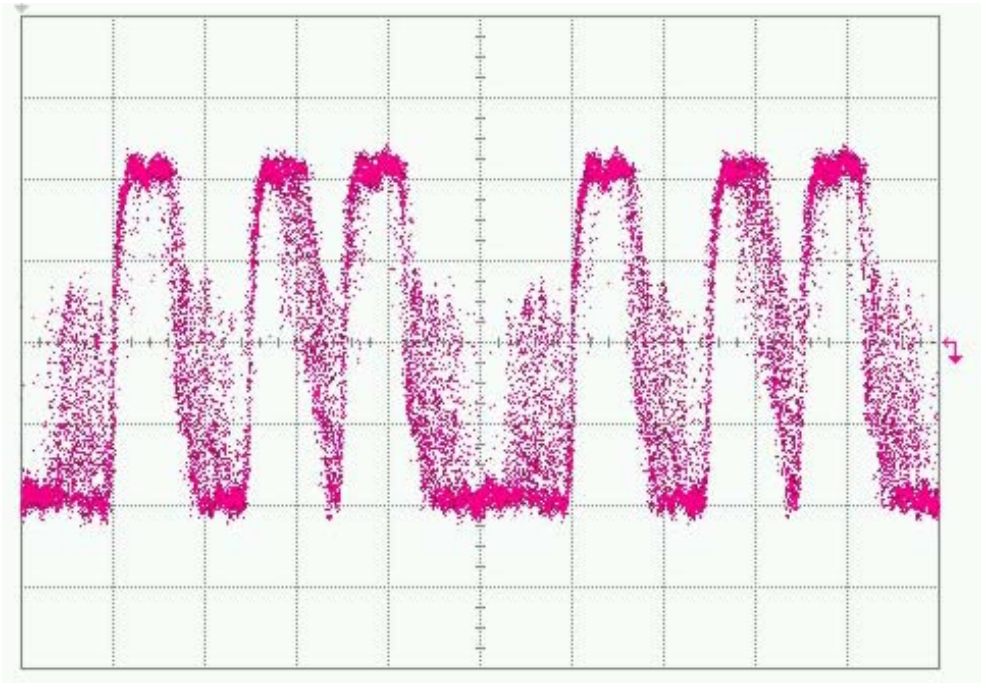

Figure 77: Single ended output (OUT+) measurement of the receiver circuit board. The input clock is 100 MHz. Voltage and time step length of 100 mV and 2 ns. The small arrow to the right is the ground level.

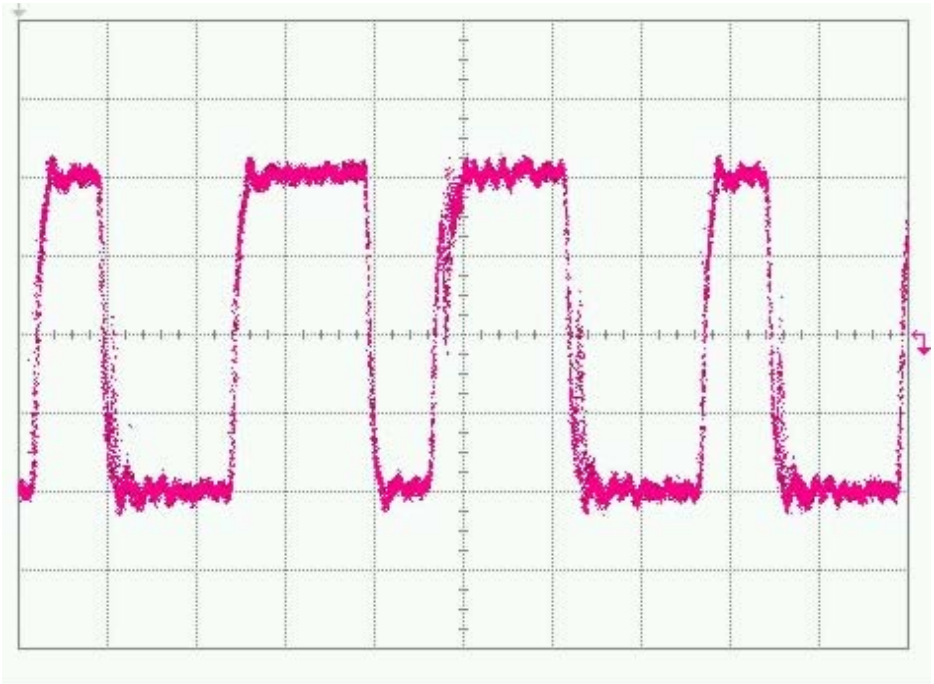

Figure 78: Single ended output (OUT+) measurement of the receiver circuit board. The input clock is 66.7 MHz. TX0-TX9 set to 1001101100 Obs. Voltage and time step length of 100 mV and 2 ns. The small arrow to the right is the ground level.

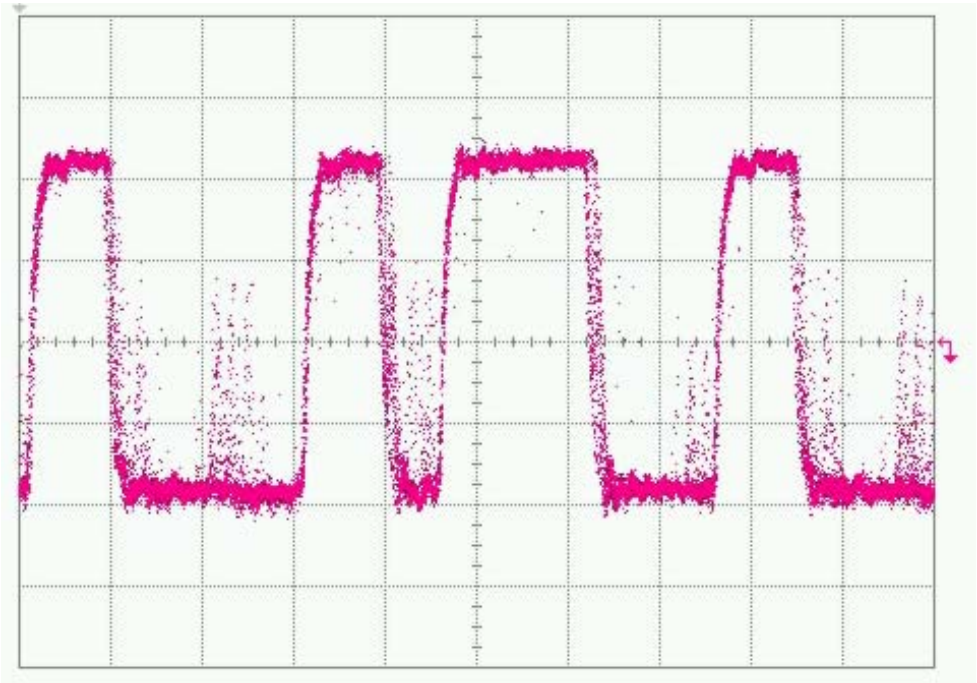

Figure 79: Single ended output (OUT+) measurement of the receiver circuit board. The input clock is 66.7 MHz. TX0-TX9 set to 1011101100 Obs. Voltage and time step length of 100 mV and 2 ns. The small arrow to the right is the ground level.

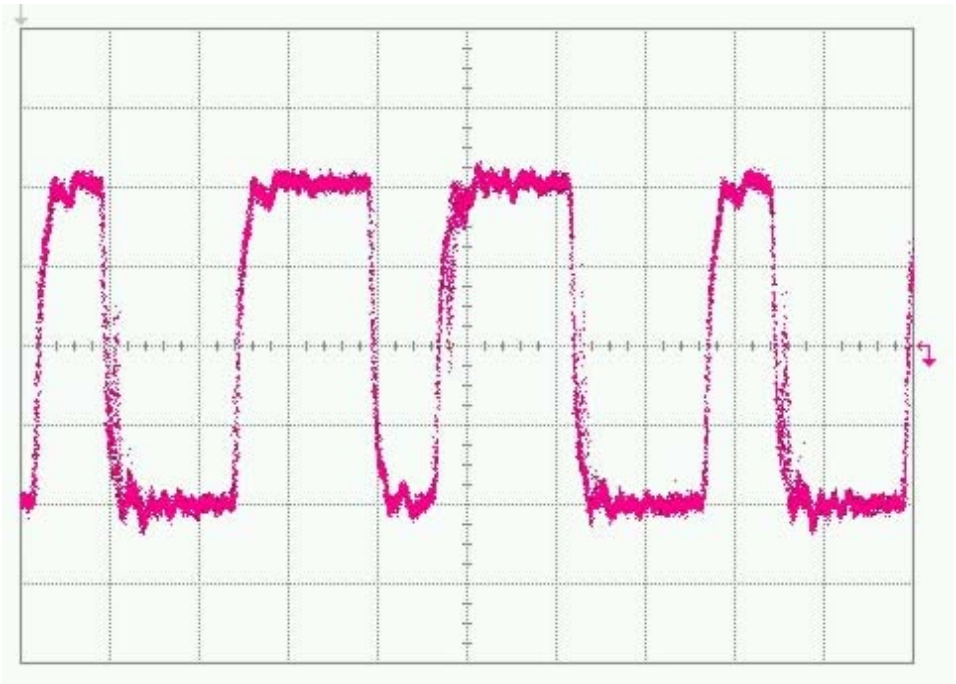

Figure 80: Single ended output (OUT+) measurement of the receiver circuit board. The input clock is 100 MHz. Voltage and time step length of 100 mV and 2 ns. The small arrow to the right is the ground level.

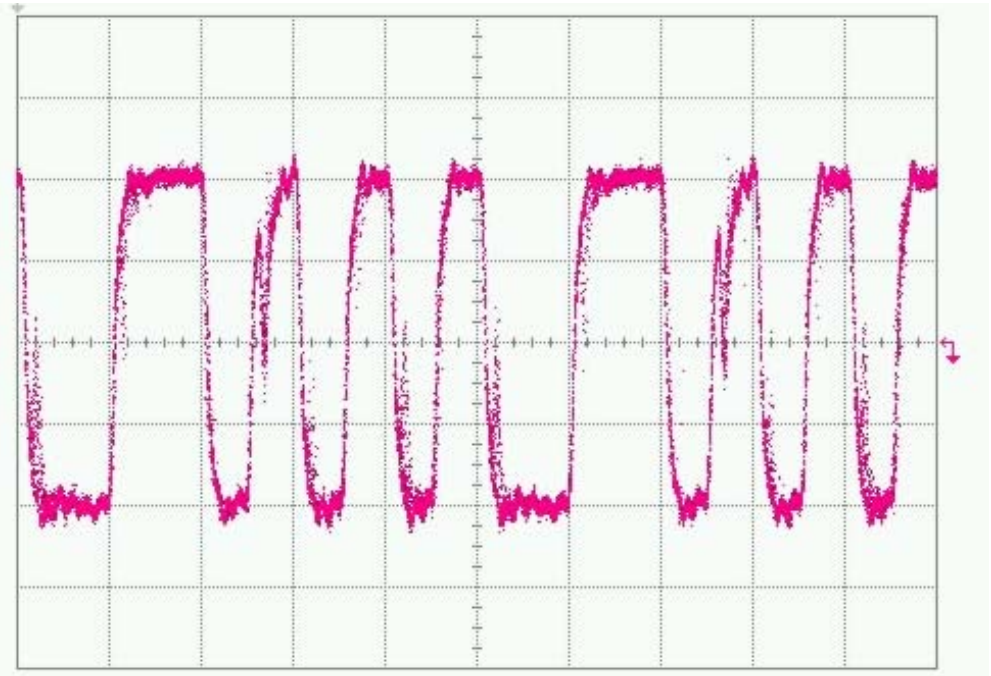

Figure 81: Single ended output (OUT+) measurement of the receiver circuit board. The input clock is 100 MHz. Voltage and time step length of 100 mV and 2 ns. The small arrow to the right is the ground level.

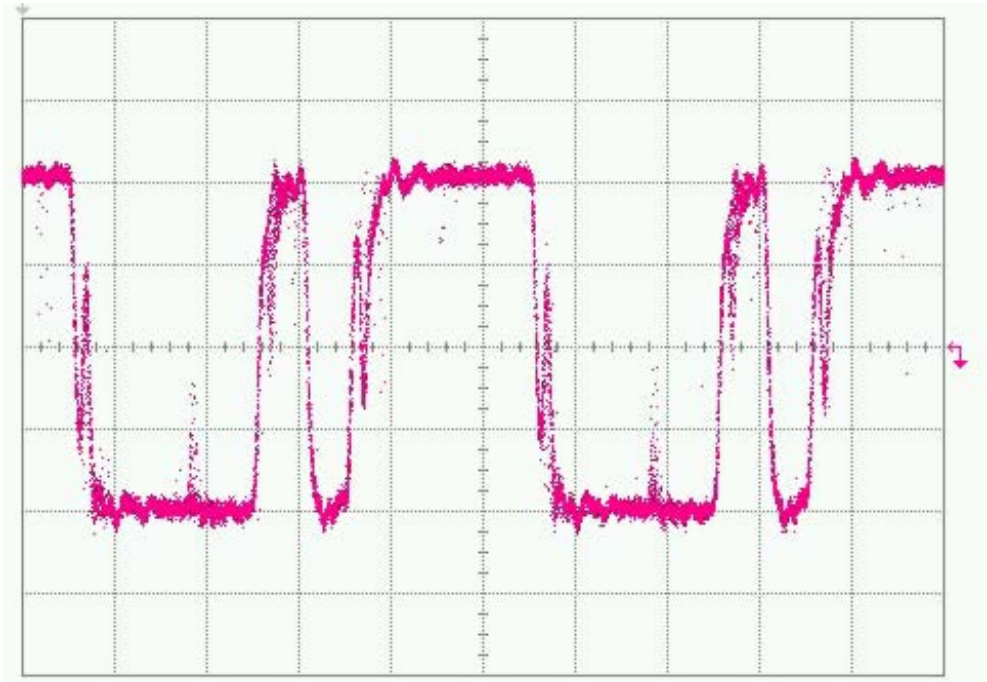

Figure 82: Single ended output (OUT+) measurement of the receiver circuit board. The input clock is 100 MHz. Voltage and time step length of 100 mV and 2 ns. The small arrow to the right is the ground level.

5. Manufacturing

There are three main steps followed in the design and manufacturing of the complete circuit boards:

- Schematic and layout design in the software Advanced Design System
- Milling of copper laminates
- Soldering

Layouts of the manufactured circuit boards can be seen in appendix A.

5.1. Circuit design in ADS

To design the circuit boards, Agilent's computer program, Advanced Design System (ADS) is used. This program is mainly used to design and simulate microwave electronic circuits, but is suitable software for usual electronic circuit design and simulation. When designing a circuit board in ADS the main steps are as follows:

- Schematic design
  Schematic design in ADS is simple. It basically consists of placing components and connecting them by wires. Many components are available in ADS and the components not available can be imported. Those components not available can be designed in the software.
- Layout design
  In layout design the layers of the circuit board is created. When designing the layout several factors must be considered, such as the trace length, component placements and milling tools available. In Figure 83 is a layout design of a component footprint (seen in Figure 84) used on the circuit boards.

A layout can be designed with or without the use of a schematic design. Part by part of the components from the schematic design can be imported to the layout design (and vice versa) to simplify design. This also minimizes design errors like misplacement of components and traces. When designing circuits with lots of traces it is highly advisable to combine schematic and layout design.

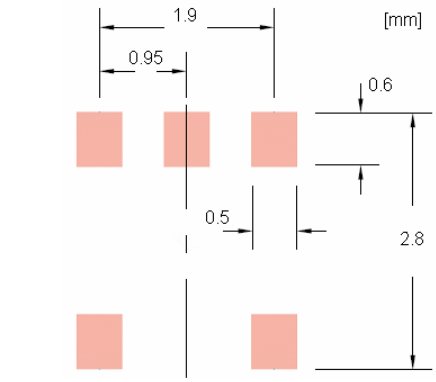

Figure 83: Footprint used in the layout of the SOT23 package.

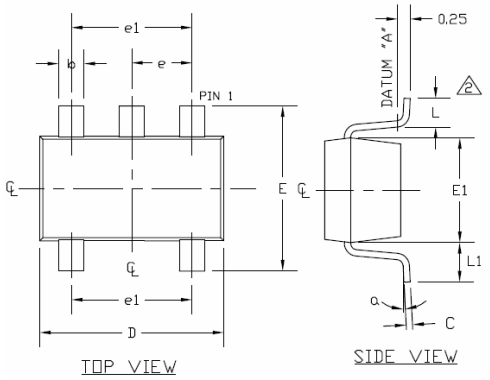

Figure 84: Outline of SOT23 package[i]. The dimensions can be found in the datasheet [30].

5.2. Milling

The milling machine, Protomat S62, is used to mill and drill the circuit boards. The material used is copper laminates that has a thin top and bottom layer of copper and a dielectric between. This makes it possible to manufacture two layer circuit boards. To mill a circuit board, the layout file from ADS must be exported to a file format[ii] that can be read by the software of the milling machine. The tool used to cut all the traces is a universal conical cutter. This cutter is designed to cut track widths of ~0.20 mm. This thickness is used in all designed circuit boards in the thesis. To drill holes, drills are used if the holes have the same diameter as the drill, otherwise mills are used. The selection of drills or mills is automatic.

5.3. Soldering

A pick-and-place tool is used to place the small surface mounted components on the circuit boards. Before component placement soldering paste was applied to designated places on the circuit boards. The by hand controlled pick-and-place tool utilizes a small needle that holds a component with a vacuum and then releases it on its designated position. With the use of a microscope and the pick-and-place tool, components can be placed on the circuit board with high precision. However, the precision is not close to perfect which makes it hard to place small components like the VCSEL driver (LTC5100) and components with many pins, like the serializer (TLK1201AI). After placement of the components the circuit boards were inspected by microscope to assure correct placement. If component placement were satisfactory, the circuit boards were heated by a heating plate to solder the components. The heating plate was at first heated at full power, to a temperature of ~170 ºC with the circuit boards lying on the plate. When this temperature was reached the heating plate was turned off and the circuit board was closely observed. The temperature of the heating plate continued to rise, and when all the soldering paste had melted, the circuit board was removed.

All components not surface mounted were soldered by hand. The front and back side of the circuit board's vias are connected by a soldered short trace (cut from a resistor or capacitor leg) and soldered by hand. All supply voltages to the circuit boards are connected by soldered wires.

[i] Footprint to the MAX4305, MAX4304 and LT1763 described in section 4.1.3
[ii] Gerber used in the thesis

6. Discussion

6.1. High speed system

The circuit boards designed are a first step towards a full-fledged system and currently an acceptable BER is potentially not reached at 1 Gbit/s. However, this is not a serious problem. In a next design phase with multilayer boards, smaller passive components and smaller vias, an acceptable BER will almost certain be reached. According to the test results in section 4.2.2 the system proves to be working all the way from serializer to receiver. However, the LA's output is distorted, due to improper grounding of its SMA contacts. The serializer circuit board seems in the tests (section 4.2.2.2) to have an almost perfect output signal all the way up to 1.3 Gbit/s.

The choice of all the components is a time demanding task. This implies that during the finite time available for this thesis it is impossible to select and evaluate all available components. Additional studies can be made in order to find the "perfect" components e.g. the best combination of laser and PIN or APD. The selected components work as is demonstrated in the thesis. If another manufacturing round is done, with better grounding for the SMA connector shields, there will be little or no problem in obtaining an almost noiseless signal at 1 Gbit/s. To increase the SNR of an APD it is suggestible to operate at the optimum gain (described in section 2.4.3.3).

6.1.1. Serializer circuit board and clock circuit

In the serializer measurement at 1 Gbit/s (Figure 70 and Figure 71) and 1.3 Gbit/s (Figure 72 and Figure 73) almost no noise is visible. The only distortion of the signal compared to a perfect square signal is some "ringing", especially at the one voltage level. However, this is probably a specific characteristic of the TLK1201AI component and is thus not possible to minimize by changing anything in the circuit board design.

The measured signal of the clock circuit (Figure 68) looks very good. The transition time is fast (~1 ns) and little noise is visible. One result that is clearly visible is that the high time (~8 ns) is significantly longer than the low time (~3 ns). Because of the difference in high and low time, operation of the serializer in DDR mode, with this clock signal, may not be possible. To be sure that operation in DDR mode is possible, the output setting of the clock circuit must be changed or the clock circuit must be exchanged to another component. However, because the clock circuit is fast enough, there are no or little reasons to operate the serializer in the lower clock speed DDR mode.

6.1.2. High speed transmitter

The selection of the laser driver LTC5100 seems to be a very good choice. The easy and fast setting of various parameters, on chip temperature sensor, on chip monitoring of critical parameters and low passive component count makes this by far the best laser driver found in the market survey performed during this thesis.

Overall, the circuit board is designed as suggested in the datasheet. However, some potential obstacles in the designed high speed transmitter may pose a problem:

- The output of the laser driver is not matched perfectly with the VCSEL. This may be a problem as described in section 2.3.1.8. A 50 Ohm resistor is connected between the pins SRC and MODA. To optimize matching the value of the VCSEL's series resistance[i] (described in 2.3.1.8) should be used. However, it may be no problem because the laser is placed so close to the laser driver.
- The grounding of the LTC5100 is not implemented as suggested in the datasheet. Several vias connected to the exposed pad[ii] is suggested. In the thesis design none of these are used.
- Larger sized passive components than suggested in the datasheet are used in the circuit board.

6.1.3. High speed receiver

There are small differences between the designed circuit board and a "perfect" receiver, designed with the same components. However, there are still some differences that may affect the performance:

- Large passive components are used on the circuit board. Smaller passive components may increase performance.
- The grounding of the SMA ports must be made properly. At the time it is not known if this "bad" grounding is due to improper circuit design or bad soldering. But it is more likely that bad soldering is the cause.
- Use of multi-layer board instead of the used double-sided PCB.

6.1.4. APD and PIN

The choice of using the combination of short wavelength laser and Si detectors is a better choice than a longer wavelength selection. No direct drawback of using a shorter wavelength has been found. Only good characteristics like low dark current compared to components based on Ge and InGaAs materials (Table 1). An improvement to the design towards less radiation complex behaviour (Appendix C) implies the usage of PINs.

6.1.5. VCSEL

The choice of VCSEL seems to be the best and most obvious selection among other types of semiconductor lasers. The good temperature behaviour, good reliability, high speed, low relaxation resonance, excellent jitter characteristic, low bias and low modulation current (described in 2.3) makes them superior.

To minimize jitter and thus increase BER, the pulse zero level (I0) should be close to threshold. This minimizes turn on delay (section 2.3.1.6). The value of I0 can be set when an acceptable turn on delay is decided. However, the selection of I0 must also take into account the change of the threshold current and output power due to temperature variations (section 2.3.1.1 and 2.3.1.3). The pulse one level current (I1) should not be selected too low. If so, it lowers the ER and

[i] 50 Ohm typical value, 90 Ohm maximum value (25 ºC, I = 4 mA) [PM67 Datasheet]
[ii] Grounded pad on the bottom of the chip

worsens the sensitivity to temperature variations and lifetime degradation, the highest possible speed of the VCSEL is also not reached (section 2.3.1.8). For the FSO system operating at 1 Gbit/s, relaxation resonance is no serious problem and can in most cases be ignored.

The selection of wavelength does not seem to influence overall performance of the system. At least no performance difference is known after the completion of this thesis. It seems likely that the only important parameter is to select a wavelength that matches the responsivity of the photodiode.

6.2. Low speed system

According to the tests in 3.3.2 and 3.3.3, the low speed transmitter and receiver operate as expected and the low speed transmitter seems to be a suitable driver for the VCSELs PM67 and PH85. However, the feedback capacitor in the receiver should be optimized. The spikes visible in the simulation (section 3.2.1) can be minimized in by increasing the rise and fall times of the bit sequence source and connecting a capacitor between the collector of the BJT and ground. This can be seen when comparing Figure 28, Figure 29 and Figure 30. The spikes are not visible in the measurement; this may be because the rise and fall times are not fast enough (~20 ns).

7. Conclusions

It has been shown that the high speed transmitter and receiver works; at least to the extent that a digital signal at 1 Gbit/s is transferred between them. The serializer circuit board has excellent performance; the measured output signal (section 4.2.2.2) seems to be almost perfect with a low noise level. Because the transmitter and receiver are tested together (section 4.2.2.3), it is not known how the high speed transmitter and receiver work separately. It is possible that the output signal of the VCSEL is almost completely noiseless compared to the measured signal in section 4.2.2.3.

As can be seen in the measurement in Figure 77 the signal is distorted by noise. This noise could be greatly minimized by adjusting the SMA outputs (SMA3 and SMA4 in Figure 49) by hand. These signals with less noise can be seen in Figure 78 to Figure 82. However, a spike-like distortion of the signal is visible shortly (~300 ps) after some transitions. This distortion is mainly visible in Figure 81 and Figure 82 but can also be seen in Figure 78 and Figure 80. The reason for this spike-like distortion is not fully understood.

The choice of VCSEL seems to be the best and most obvious selection over other types of semiconductor lasers. The good temperature behaviour, good reliability, high speed, low relaxation resonance, excellent jitter characteristic, low bias and low modulation current (described in 2.3) makes them superior.

A suggestion of the modulation of the VCSEL is that the pulse zero level (I0) should be close to threshold. This minimizes turn on delay (section 2.3.1.6). The value of I0 to use can be set when an acceptable turn on delay is decided. However, the selection of I0 should also take into account the change of the threshold current and output power due to the change in temperature (section 2.3.1.1 and 2.3.1.3). The pulse one level current (I1) should not be selected too low. This not only lowers ER but also worsens the sensitivity to temperature variations and lifetime degradation, the highest possible speed of the VCSEL is also not reached (section 2.3.1.8). For the FSO system operating at 1 Gbit/s, relaxation resonance is no problem and can in most cases be ignored.

The low speed transmitter and receiver are demonstrated to operate as intended, but the feedback capacitor for the low speed receiver should be exchanged to another value (described in section 3.1.4.2) to minimize the ringing and improve speed response.

8. Future work

For a final system that is operational in space, the system must be protected against radiation and optimized for low power consumption. A possibility for the final transmitter is to read and control the laser driver's (LTC5100) parameters from Earth, while the system is in space. Temperature compensation and the MPC[i] availability of the laser driver is not used in this thesis design and these are great tools in controlling the output power of the VCSEL, especially in space where the temperature can vary a lot. Use of temperature compensation should preferable be incorporated in a final transmitter module. The use of MPC must be further investigated due to the change in ER and turn-on delay (described in 2.3.1.9).

The use of either APD or PIN needs further investigations. It must be decided if the worse temperature properties, much higher bias voltage, higher power consumption and less predictable radiation properties are worth the signal gain of the APD compared to the PIN. In the presented design, switching between APD and PIN is not especially time demanding since the change in circuit design is minimal, especially if a combined PIN/TIA component is used. A suggestion of a PIN/TIA chip is the FCI-H125G-010. If it is decided to not use a combined PIN/TIA a possible TIA candidate is the circuit ADN2880, MAX3744 or MAX3745. The temperature characteristics of the used TIA/APD chip AD500 is not satisfactory stated in the datasheet. So, investigation of this temperature behaviour is suggested. A version of the AD500-1.3G-TO5 (named AD230-2.3G-TO5) with a smaller active area is available. This circuit has an active area diameter of 230 μm and a higher bandwidth. This chip is packaged as the AD500 and can thus be directly soldered to the high speed receiver circuit board.

The choice of active area of the photodiode must also be investigated. A smaller active area means less noise and lower terminal capacitance, but then the input signal will be lower. If selecting an APD, feedback to stabilize the gain or some kind of temperature stabilization must be incorporated, because the temperature can vary a lot in a spacecraft. The properties of materials other than Si, Ge and InGaAs can be investigated.

To complete the electronics a clock and data recovery (CDR) and deserializer circuit should be incorporated. No suitable CDR chip was found during the thesis work, but a suitable combined LA and CDR chip may be ADN2813 or ADN2812. The CDR circuit investigated in the thesis work is Micrel's chip SY87701AL. Unfortunately, this chip has not a high enough TTL[ii] input high voltage when operated with the MAX3748. Using an extra amplifier after the MAX3748, selection of another LA or finding a suitable CDR would solve this problem. As deserializer the used SERDES chip (TLK1201AI) is suggestible for simplicity. This clock buffer (CDCV304) on the serializer circuit board is not required and it should be evaluated if it should be removed to minimize circuit size.

[i] Mean Power Control
[ii] Transistor Transistor Logic

9. Acknowledgments

The following have assisted in the completion of this thesis:

• **Ångström Space Technology Center, ÅSTC:**
Hugo Nguyen: Assistant Professor
Greger Thornell: Associated Professor
Henrik Kratz: Assistant Professor

• **Swedish Institute of Space Physics, IRF:**
Farid Shiva: Engineer

• **Sponsors:**
VINNOVA Swedish Governmental Agency for Innovation Systems
SNSB Swedish National Space Board

CHAPTER 9. ACKNOWLEDGEMENTS

References

[1] – Free Space optics (FSO): An Introduction, SONA OPTICAL WIRELESS, (www.free-space-optics.org – 2008-01-22)

[2] – Free Space Optical Communications, Encyclopedia of Laser Physics and Technology, RP-Photonics, (www.rp-photonics.com/free_space_optical_communications.html – 2008-01-22)

[3] – Lasers carry space data back to Earth, Opto & Laser Europe, June 2004 (http://optics.org/cws/article/articles/19697 - 2008-02-05)

[4] – Mission operation completed with "extra success", November 2, 2006, (http://www.jaxa.jp/projects/sat/oicets/index_e.html - 2008-03-25)

[5] – Design of high-speed CMOS laser driver using a standard CMOS technology for optical data transmission, Seok Hun Hyun, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, November 2004

[6] – Prospects of CMOS technology for High-Speed Optical Communication Circuits, Behzad Razavi, Senior Member, IEEE, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 37, NO. 9, SEPTEMBER 2002

[7] – Transimpedance Amplifier Design using 0.18 um CMOS Technology, Ryan Douglas Bespalko, Queen's University, Kingston, Ontario, Canada, July 2007

[8] – Vertical Cavity Surface-emitting Lasers, Encyclopedia of Laser Physics and Technology, RP-Photonics, (http://www.rp-photonics.com/vertical_cavity_surface_emitting_lasers.html - 2008-02-05)

[9] – Modulating VCSELs, Application note, Finisar Advanced Optical Components Division, 01/07

[10] – Understanding Optical Communication, Harry J. R. Dutton, SG24-5230-00, IBM

[11] – http://en.wikipedia.org/wiki/Photodiode - 2007-10-12

[12] – Optical Communications, Telecommunication Engineering, School of Engineering, University of Rome La Sapienza, Rome, Italy, 2005-2006

[13] – http://www.masbonfante.it/english/cards/scheda_gpd.htm - 2008-03-05

[14] – Choosing the Detector for your Unique Light Sensing Application, Larry Godfrey, PerkinElmer

[18] – Physics and technology, Emitters, Vishay Semiconductors, Document Number: 80113

[20] – Photodiode Technical Information, Hamamatsu, (http://sales.hamamatsu.com/assets/applications/SSD/photodiode_technical_information.pdf - 2008-09-24)

[21] – Characteristics and use of Si APD (Avalanche Photodiode), Hamamatsu, – Cat. No. KAPD9001E03, May 2004 DN

[22] – Si APD, S6045 series, Hamamatsu, Cat. No. KAPD1005E03, Mar. 2001DN

[23] – Compensate Transimpedance Amplifiers Intuitively, Tony Wang, Barry Erhman, Texas instruments, Application Report SBOA055A–March 1993–Revised March 2005

[24] – http://www.optowell.com/homepage2/code.html – 2008-02-29

[25] – Maxim, Engineering Journal, Volume Thirty-Four (http://pdfserv.maxim-ic.com/en/ej/EJ34.pdf - 2008-03-04)

[26] – http://cp.home.agilent.com/upload/cmc_upload/U2356A_800x407.jpg

[27] – http://en.wikipedia.org/wiki/SMA_connector - 2008-02-15

[28] – LTC5100, 3.3V, 3.2Gbps VCSEL Driver, sn5100 5100fs, LT/TP 0903 1K • PRINTED IN USA, LINEAR TECHNOLOGY CORPORATION 2003

[29] – TLK1201ARCP, TLK1201AIRCP, ETHERNET TRANSCEIVERS, SLLS580D–FEBRUARY 2004–REVISED SEPTEMBER 2007

[30] – Package SOT23 Maxim, Document Control No. 21-0057

[31] – Simulation of silicon PIN photodiodes for use in space-radiation environments, M A Cappelletti, A P C´edola and E L Peltzer y Blanc´, Received 14 August 2007, in final form 20 November 2007 Published 4 January 2008, Semicond. Sci. Technol. 23 (2008) 025007 (7pp)

[32] – The Influence of Structural Characteristics on the Response of Silicon Avalanche Photodiodes to Proton Irradiation, Heidi N. Becker, Tetsuo F. Miyahira, Member, IEEE, and Allan H. Johnston, Fellow, IEEE

[33] – Bit Error Rate: Fundamental Concepts and Measurement Issues, Gary Breed, From January 2003 High Frequency Electronics Copyright © 2003 Summit TechnicalMedia, LLC

[34] – Bit-Error Rate (BER) For High-Speed Serial Data Communication, Palani Subbiah, Cypress Semiconductor, Data-communication Division

[35] – Jitter–Understanding it, Measuring It, Eliminating It Part 1: Jitter Fundamentals, Johnnie Hancock, Agilent Technologies, From April 2004 High Frequency Electronics, Copyright © 2004 Summit Technical Media, LLC

[36] – Analyzing Signals Using the Eye Diagram, Gary Breed, November 2005, High Frequency Electronics, Copyright © 2005 Summit Technical Media

[37] – Measuring Deterministic Jitter with a K28.5 Pattern and an Oscilloscope, HFAN-4.5.0, Rev 0; 07/02.

[38] – http://en.wikipedia.org/wiki/Laser_safety - 2007-10-22

[39] – http://en.wikipedia.org/wiki/Optical_density - 2008-03-26

[40] – http://en.wikipedia.org/wiki/Optical_density - 2007-10-22

[41] – PM67-F1P0N, 670 nm VCSEL TO46 Can Package, Rev. 1.0

REFERENCES

Appendix A

In this appendix, the layouts of the designed circuit boards are shown.

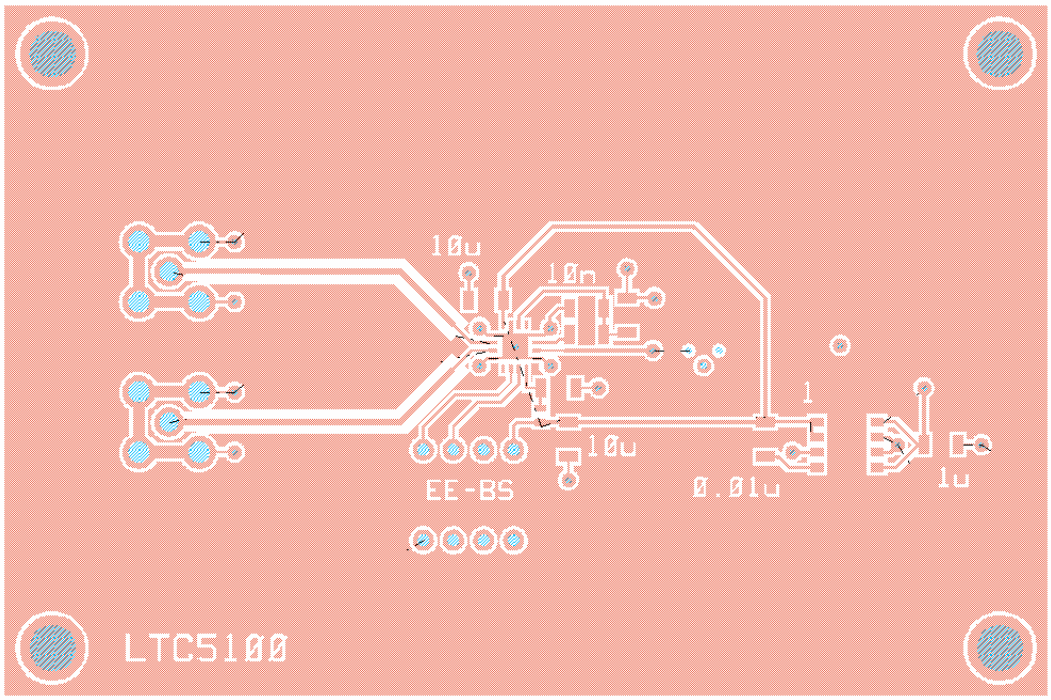

Figure A - 1: Top layer of the high speed transmitter. Size of board: 88 mm x 58 mm.

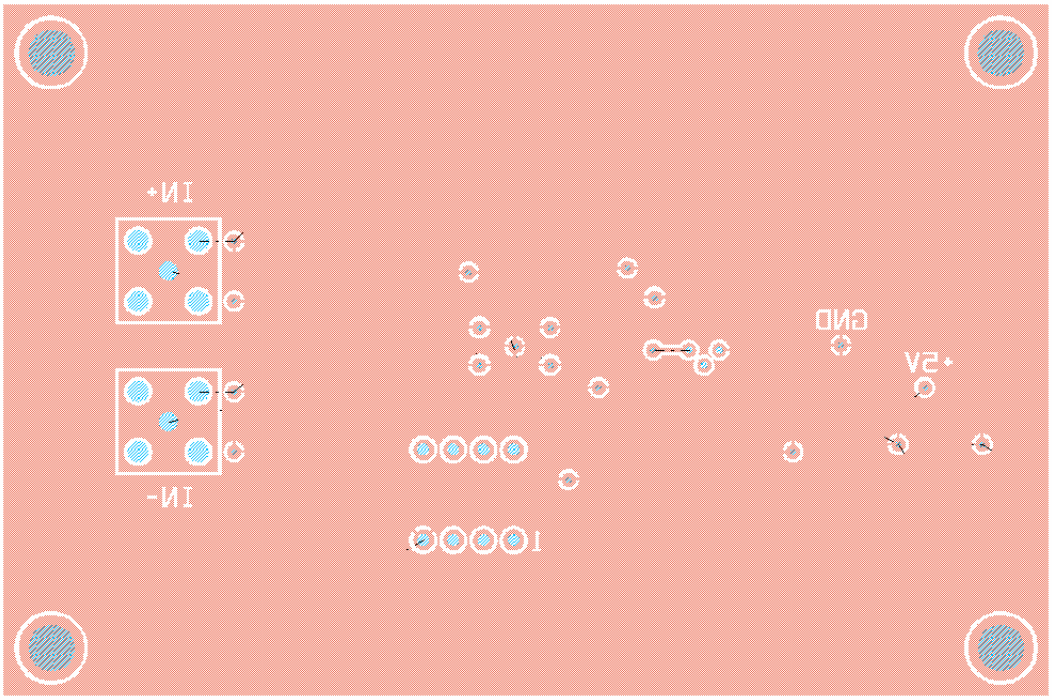

Figure A - 2: Bottom layer of the high speed transmitter.

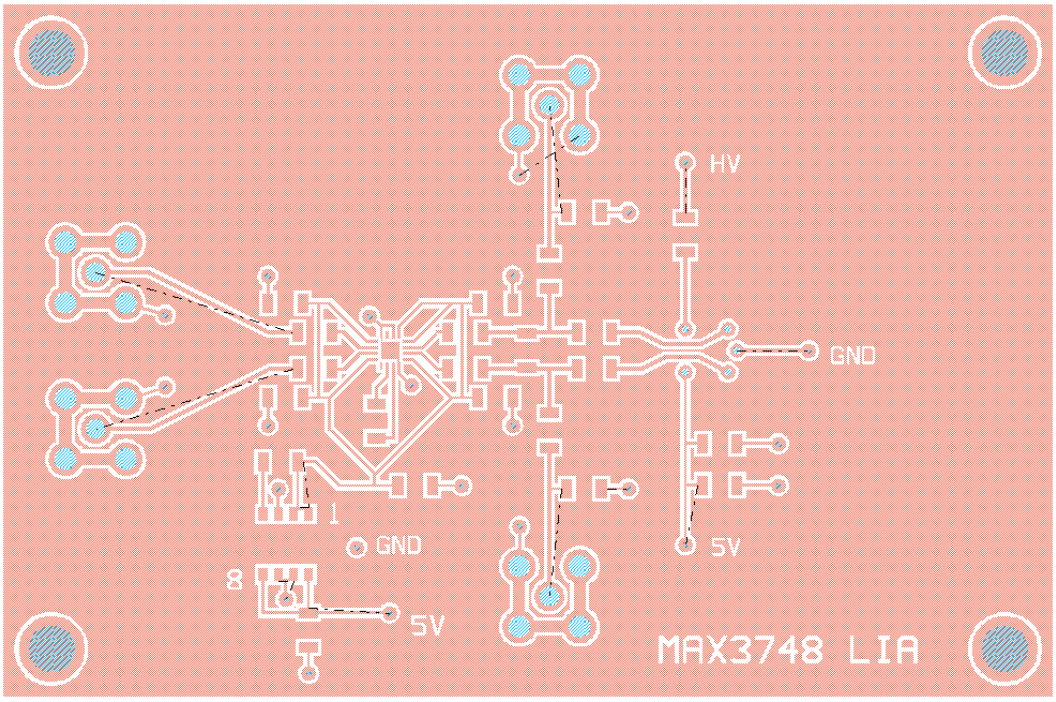

Figure A - 3: Top layer of the high speed receiver. Size of board: 88 mm x 58 mm.

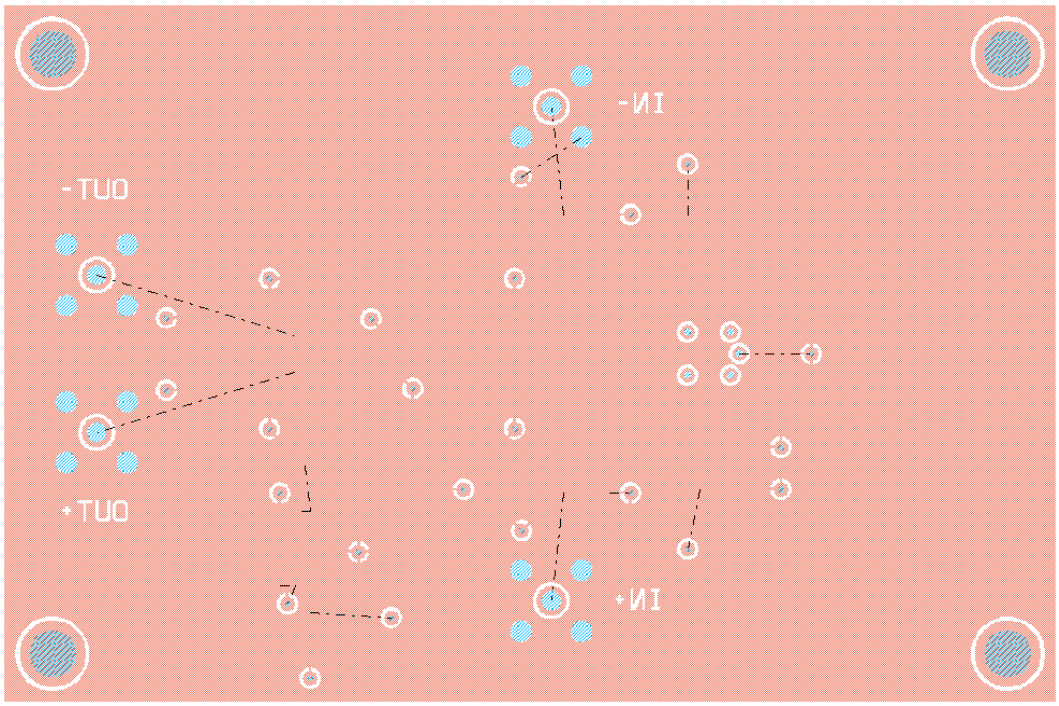

Figure A - 4: Bottom layer of the high speed receiver.

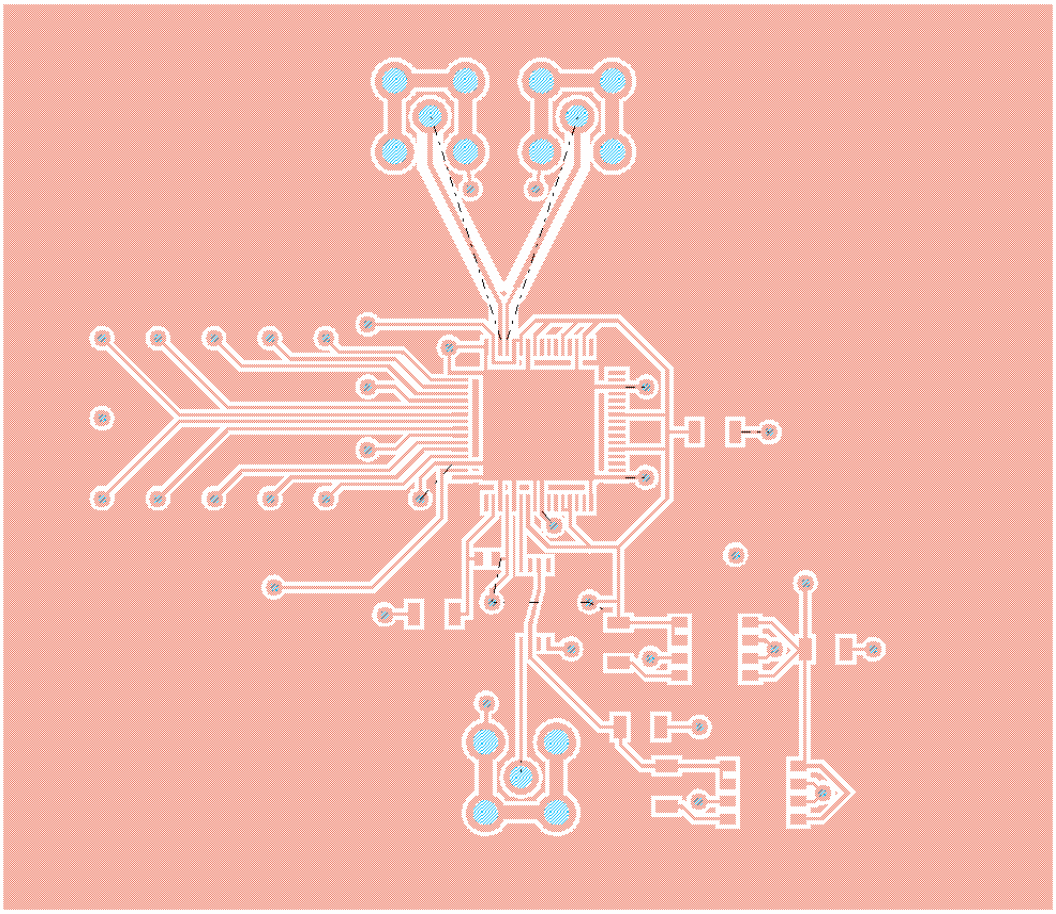

Figure A - 5: Top layer of the serializer circuit board. Size of board: 75 mm x 65 mm.

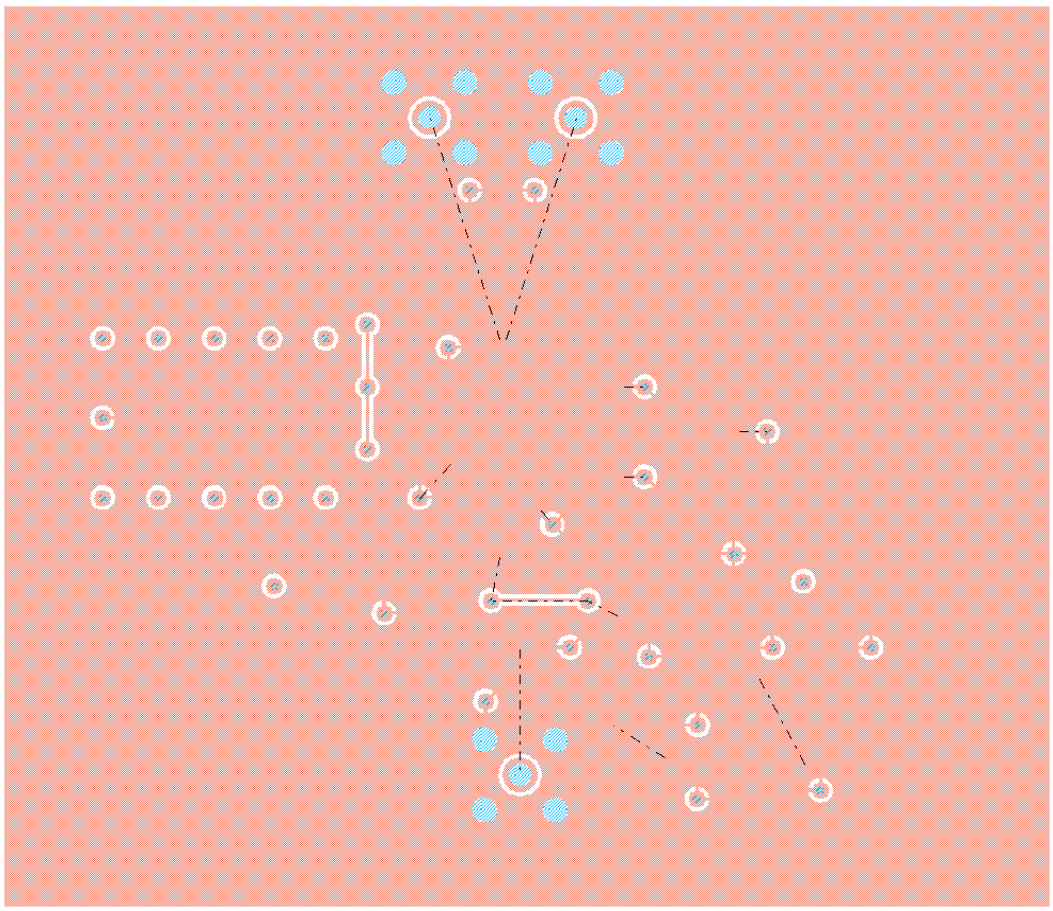

Figure A - 6: Bottom layer of the serializer circuit board.

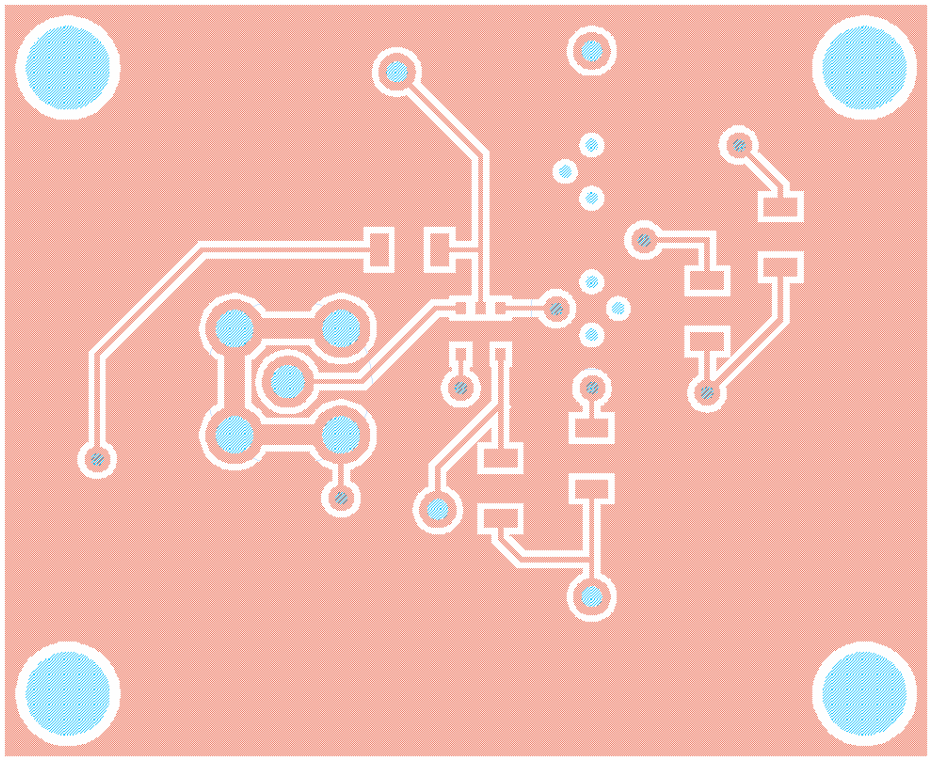

Figure A - 7: Top layer of the low speed transmitter. Size of board: 44 mm x 35.9 mm.

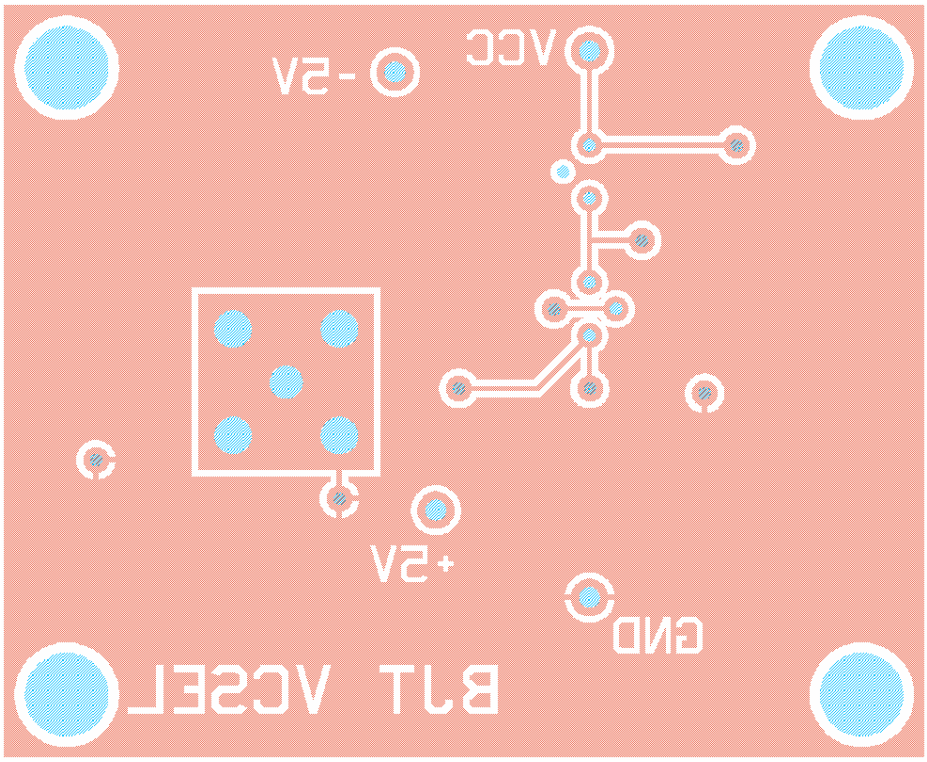

Figure A - 8: Bottom layer of the low speed transmitter.

APPENDIX A

Appendix B

In this appendix step-by-step rewriting from the selected values in the LTC5100's memory map too hexagonal numbers (required by the pikprog2's bundled software) of the laser driver's parameters is shown.

Table B - 1: LTC5100's EEPROM memory map. [28]

	7	6	5	4	3	2	1	0
15	Reserved			Peaking (4:0)				
14	Ib_gain(4:0)					Im_gain(2:0)		
13	Reserved				Imd_rng(1:0)		T_nom(9:8)	
12	T_nom(7:0)							
11	Im_tc2(7:0)							
10	Im_tc1(7:0)							
9	Reserved				Im_rng(1:0)		Im_nom(9:8)	
8	Im_nom(7:0)							
7	Ib_tc2(7:0)							
6	Ib_tc1(7:0)							
5	Reserved				Is_rng(1:0)		Ib_nom(9:8)	
4	Ib_nom(7:0)							
3	Reserved				Rep_flt_inhibit	Rapid_restart_en	Flt_drv_mode	
2	Lpc_en	Auto_shutdn_en	Flt_pin_polarity	Flt_pin_override	Force_flt	Over_pwr_en	Under_pwr_en	Over_current_en
1	Reserved	Ib_limit						
0	Cml_en	Md_polarity	Ext_temp_en	Power_down_en	Apc_en	En_polarity	Soft_en	Operating_mode

Table B - 2: LTC5100's EEPROM memory with selected values.

	7	6	5	4	3	2	1	0
15	Reserved			16				
14	16					4		
13	Reserved				0		0	
12								
11	0							
10	0							
9	Reserved				0		227	
8								
7	0							
6	0							
5	Reserved				1		227	
4								
3	Reserved				0	1	1	1
2	1	1	1	0	0	0	0	0
1	Reserved	0						
0	1	0	0	1	0	0	1	0

Table B - 3: LTC5100's EEPROM memory with selected values in binary.

	7	6	5	4	3	2	1	0
15	Reserved			10000				
14	16					100		
13	Reserved				0		0	
12								
11	0							
10	0							
9	Reserved				0		11100011	
8								
7	0							
6	0							
5	Reserved				1		11100011	
4								
3	Reserved				0	1	1	1
2	1	1	1	0	0	0	0	0
1	Reserved	0						
0	1	0	0	1	0	0	1	0

Table B - 4: Table B - 3 rewritten with each binary number in one memory spot. Zeros set as reserved.

	7	6	5	4	3	2	1	0
15	0	0	0	1	0	0	0	0
14	0	0	0	0	1	1	0	0
13	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	1	1
8	1	0	0	0	1	1	0	0
7	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
5	0	0	0	0	0	1	1	1
4	1	0	0	0	1	1	0	0
3	0	0	0	0	0	1	1	1
2	1	1	1	0	0	0	0	0
1	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	1	0

Table B - 5: Table B - 4 rewritten to two columns.

	7::4	3::0
15	1	0
14	0	1100
13	0	0
12	0	0
11	0	0
10	0	0
9	0	11
8	1000	1100
7	0	0
6	0	0
5	0	111
4	1000	1100
3	0	111
2	1110	0
1	0	0
0	1001	10

Table B - 6: Table B - 5 rewritten with hexagonal numbers.

	7::4	3::0
15	1	0
14	0	C
13	0	0
12	0	0
11	0	0
10	0	0
9	0	3
8	8	C
7	0	0
6	0	0
5	0	7
4	8	C
3	0	7
2	E	0
1	0	0
0	9	2

BUFFPRN

```
;--- Buffer dump
PG4UW - universal program for Elnec programmers, version 2.46/01.2008
Date: 14.februari 2008  Time: 11:19:52
Selected device: Microchip  24LC00

Buffer content from address: 00000000h, to address: 0000010Fh

Address      +0 +1 +2 +3 +4 +5 +6 +7 +8 +9 +A +B +C +D +E +F  0123456789ABCDEF
-------------------------------------------------------------------------------
0000000000   92 00 E0 07 8C 07 00 00 8C 03 00 00 00 00 0C 10  '.à.Œ...Œ.......
0000000010   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0000000020   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0000000030   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0000000040   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0000000050   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0000000060   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0000000070   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0000000080   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
0000000090   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
00000000A0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
00000000B0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
00000000C0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
00000000D0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
00000000E0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
00000000F0   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ

0000000100   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF  ÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿÿ
```

Figure B - 1: Settings of the EEPROM of the laser driver LTC5100. Printed from ELNEC's software PG4UW. The first row (Adress 0000000000) is the settings of the physical memory.

APPENDIX B

Appendix C

Photodiodes in radiation environment

It is evident that care must be used when choosing the PIN or avalanche photodiode for use in space applications. The hazardous radiation environment in space degrades all electronic devices and systems. Incident protons, heavy ions, neutrons and electrons damage semiconductors and accelerate aging of electronics. The influence of proton radiation is severe, because they are highly penetrating, are present in large numbers and are relatively massive. Proton radiation degrades semiconductors through both displacement and ionization damage and are the main source of radiation at LEO (Low Earth Orbit).

Si PIN photodiodes in radiation environment

The degradation of Si PIN photodiodes due to proton radiation seems to be dependent on the intrinsic layer thickness and the resulting degradation is an increase of dark current [31]. When a PIN photodiode isn't illuminated during radiation (of 10 MeV protons) the dark current tends to follow the formula obtained by the computer simulations in [31]

$$I_{Dark} = I_{Dark,W/R} + \alpha L_I \phi \qquad \text{(C:1)}$$

where I_{Dark} (in μA) is the dark current after the sample has been radiated, $I_{Dark,\ W/R}$ the dark current before the PIN photodiode been radiated, α is the current damage rate (α = 1.3344 x 10^{-12} μAcm^{-1} for Si), Φ is the fluence of protons in p^{+}/cm^{2} and L_I (in cm) is the intrinsic layer thickness. As can be seen in the above formula the dark current increases with the proton fluence and intrinsic layer thickness. That is, the damage suffered in the N-type and P-type regions doesn't contribute to the change in electrical characteristics in any significant way.

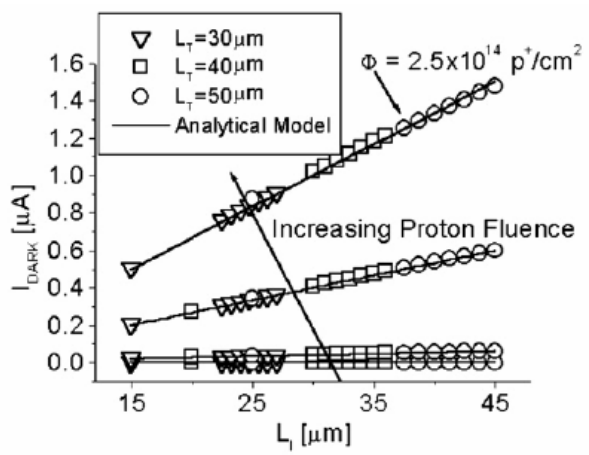

Figure C - 1: The effect on different devices dark current after irradiation by 10 MeV protons. Observe that this is results from a computer simulation. [31]

Because the photo current decreases with increased fluence, the effect on the total reverse current (photocurrent + dark current) shows a completely different behaviour. Depending on the ratio between total length and intrinsic length of the device, the total reverse current could increase, decrease or not change at all. So a specific ratio (depending on the light wavelength) between the intrinsic layer

length and the total length exists to keep a constant total reverse current. Plots of the simulated radiation effects to PINs can be seen in Figure C - 1 and Figure C - 2.

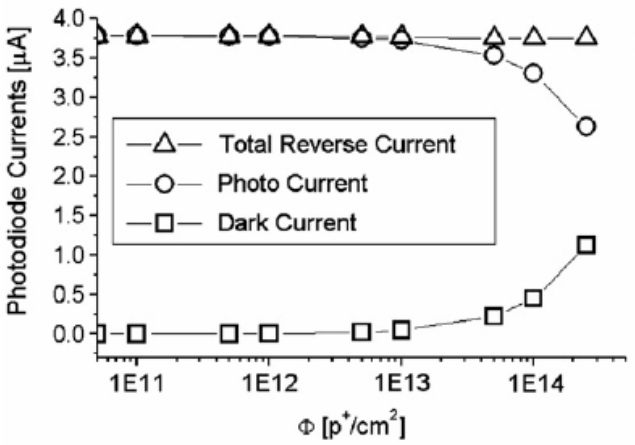

Figure C - 2: The total photo and dark current for a PIN photodiode when subjected to 10 MeV protons. During the test the diode is illuminated. The total length is 50 µm and the intrinsic layer is 32.9 µm. Observe that this is results from a computer simulation. [31]

Avalanche photodiodes in radiation environment

The effects on APDs when subjected to radiation are far more complex than the effects on PIN devices, but are similar due to the increase of dark current. After a 51 MeV proton radiation test in [32] on three different APD types, with different depletion region depth, a large increase of dark current could be measured. At low fluences the device with the longest depletion region depth, measures a one order higher dark current than the shorter depletion region depth device. The dark current increase is highly dependent on the volume of the depletion region; the higher volume the higher dark current increase due to radiation. The test also shows that the dark current increase primarily is due to displacement damage in the depletion region, and the displacement damage is directly proportional to the volume of this region, at low fluences. As can be seen in Figure C - 3, the dependence between dark current and depletion region depth breaks down at higher fluences with ~1/2 of the shallow devices measures the highest dark current.

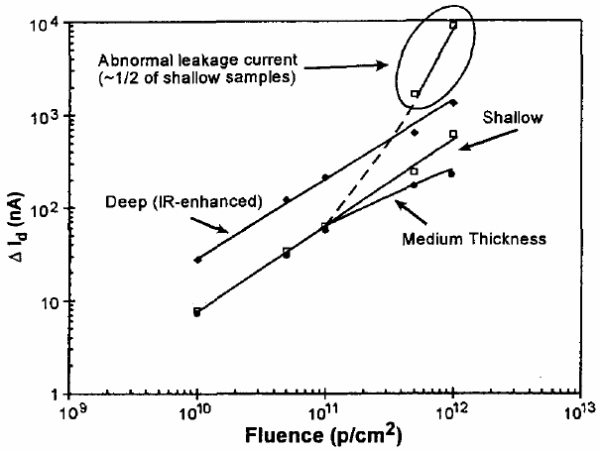

Figure C - 3: The dark current test result for different devices. Observe that ½ of the shallow samples shows an abnormal leakage current. The irradiating particles are 51 MeV protons. [32]

The change in photocurrent is also a concern. The test shows that the photocurrent decreases consistently with fluence (seen in Figure C - 4), and the loss is higher for deep and medium device than for shallow devices. At lower fluences there appears to be a relatively straight forward trade off between high photo sensitivity at longer wavelengths (long depletion width) and the damage to the device due to radiation, but the doping level and the structure of the APD also has an influence on the radiation resistance. The radiation hardness seems also to have large variances between individual devices of the same type. [32]

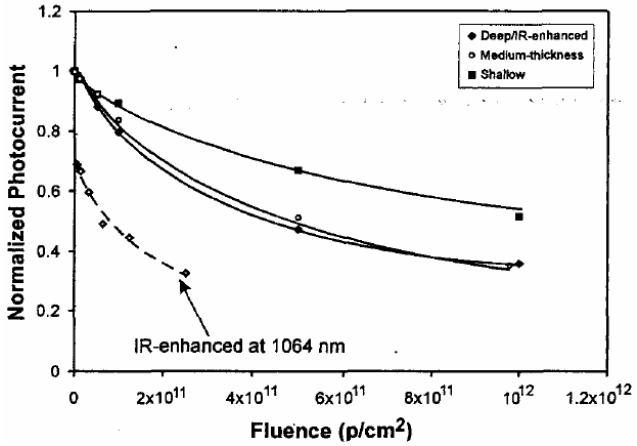

Figure C - 4: The normalized photocurrent test result for three different APD types. The irradiating particles are 51 MeV protons. [32]

APPENDIX C

Appendix D

Bit Error Rate (BER)

BER quantifies the reliability of the entire communication link from “bits in” to “bits out”. BER is defined as [33]

$$BER = \frac{Total\ \ Number\ of\ \ Errors}{Total\ \ Number\ of\ \ Bits}. \qquad \text{(D:1)}$$

The main contributor to bad BER performance is noise, but quantization error also reduces the BER performance, through incorrect or uncertain reconstruction of the digital waveform. These errors come primarily from the circuits performing analog-to-digital and digital-to-analog conversions [33]. Bit errors can be caused by random events or improper design. In optical links the errors occur primarily because of the physical components used to make the link (optical driver, optical receiver, optical fiber, etc), but errors also occurs due to optical dispersion and optical attenuation. One of the largest factors of noise-induced errors is the TIA. The small photo current from the photodiode (often less than a few µA) makes the TIA susceptible to thermal or shot noise, and converts these into random jitter (described below) [34].

Jitter can be defined as the time deviation from ideal timing of a signal transition through a decision threshold. An example of jitter in an ideal digital signal can be seen in Figure D - 1. At high speed communication design, jitter is one of the most significant design parameters. Systems operating over 1 Gbit/s must be concerned with the effects on BER by jitter [35]. Jitter can be divided into two parts, random jitter and deterministic jitter. Random jitter is caused by noise generated in the components and cannot be correlated to either data-stream contents, or parameters of the hardware. Deterministic jitter is difficult to predict and arises due to deterministic characteristics of the data stream. The misplacements of transitions can often be correlated to the content of the data stream or some specific characteristics of the circuit or hardware [34].

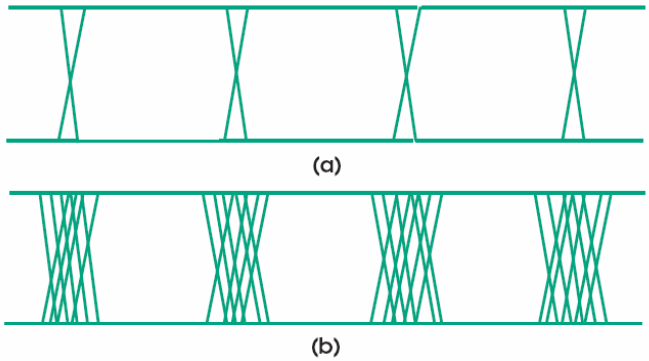

Figure D - 1: Ideal digital signal eye diagram without jitter (a) and with jitter (b). Both signals have finite rise and fall times. [36]

One way to measure jitter and other characteristics of a data link is to study the eye diagram when a specified or random data sequence is sent through the system. An eye diagram shows a merged view of multiple waveforms superimposed upon

each other. One (of many) often used standardized data sequences is the K28.5 pattern. The data sequence is a character in the 8B/10B coding table and consists of the following 20 bits: 00111110101100000101. K28.5 is supposed to represent a typical signal and is sent repeatedly [37]. The K28.5 pattern contains both 5 consecutive ones and zeros and also contains an isolated zero (101) and an isolated one (010).

An example of the basic information contained in an eye diagram is shown in Figure D - 2. The most important information in the eye diagram is the "opening of the eye" (signal-to-noise during sampling), the magnitude of the amplitude during sampling and the jitter [35]. Unfortunately the eye diagram does not allow separation of deterministic and random jitter, nor does it allow removal of jitter caused by the test system [37].

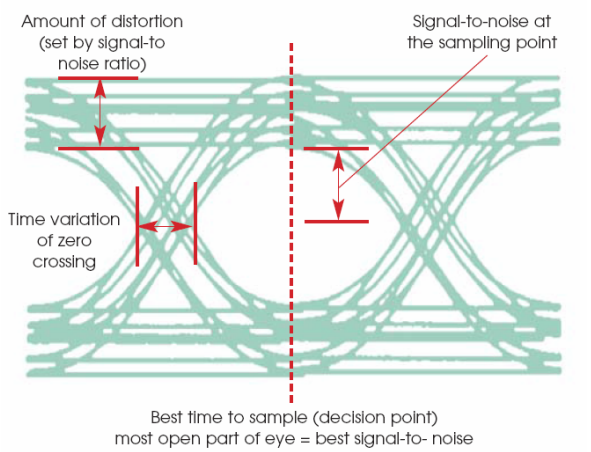

Figure D - 2: Some of the basic information extractable from an eye diagram. The time variation at the zero crossing is called jitter. [36]

Appendix E

Laser safety

Because that communication lasers are low power lasers it is widely believed that they are no threat to eye-injury. This is not true. Because lasers produce a narrow, in phase and parallel beam of concentrated light, a very low power laser can be a hazard. Many different factors of a laser influence the degree of hazard. The most obvious are light intensity, wavelength and exposure duration. A less obvious factor is the ambient light. Because the pupil opens in a darkened room, laser emission viewed in a darkened room is much more dangerous than viewed in bright sunlight. [10] If the wavelength of the laser is invisible the laser light may be more dangerous than a visible laser because one may not be able to look away when the light strikes the eye.

The two lasers, PM67 and PH85, are classified as class IIIb (3b). A class IIIb laser may cause eye damage if the beam enters the eye directly. This generally applies to laser output powers in the range of 5-500 mW. A very small exposure time (1/100 second or less) can be enough to cause permanent eye damage. Generally a diffuse reflection is not hazardous but a clean reflection is still dangerous. Eye protection is recommended when operating class IIIb lasers [38].

Protecting eyewear is usually stated in the US standard ANSI Z136, or the European standard EN 207. The US standard ANSI Z136-2 is used when operating fibre communication laser diodes [38]. The protecting property of laser protecting goggles is generally stated in optical density (OD) and is a measurement of how much the light in one specific wavelength is attenuated. OD is measured as the 10-base logarithm. A high OD value means a high protecting property. Optical density is calculated as [39]

$$OD_\lambda = \frac{A_\lambda}{l} = -\log_{10} T = \frac{1}{l}\log_{10}\left(\frac{I_0}{I}\right) \qquad \text{(E:1)}$$

where A_λ is the absorbance at wavelength λ, l the distance in cm that the light travels in the sample, T the per-unit transmittance, I_O, the intensity of the incident beam of light and I is the intensity of the transmitted light beam.

Absorbance does not have a true unit but is usually written as “Absorbance unit” (AU). Accordingly, optical density is measured in AU/cm. Optical density is sometimes stated without regard of the thickness (l) of the material. In those cases OD is a synonym for absorbance [40].

APPENDIX E

Appendix F

Schematic low speed model of the VCSELs

In order to simulate the low speed transmitter (section 3.2.1) a low speed model of the VCSELs, PM67 and PH85 is constructed. This model can be seen in Figure F - 3.The IV[i] characteristic of the VCSELs is almost the same as a "normal" diode above threshold. Because of this similarity, models of the VCSELs are constructed by using the diode model ap_dio_IDEALDIODE_19930601 (called Apdio in the following text). Apdio is integrated in ADS[ii]. The IV curves of the Apdio and PM67 (LIV[iii] curve) is shown in Figure F - 1 and Figure F - 2.

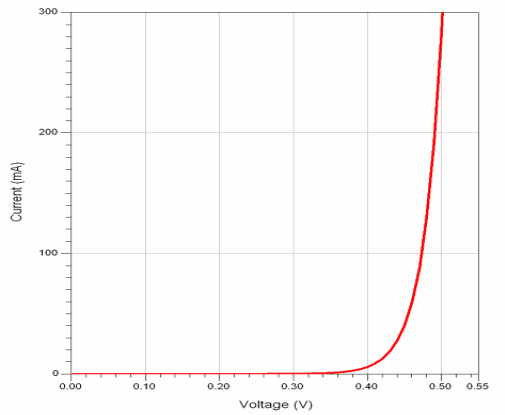

Figure F - 1: Apdio's IV curve DC swept in ADS.

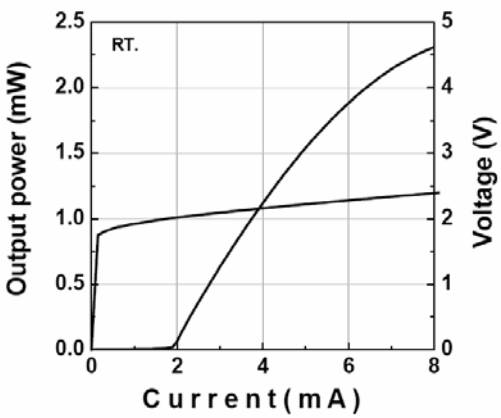

Figure F - 2: LIV curve at 25 ºC of the PM67 VCSEL. [41]

Figure F - 3: The VCSEL low speed schematic above threshold model.

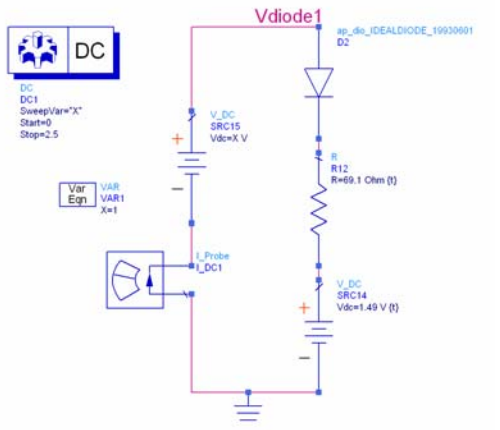

Figure F - 4: DC swept circuit.

Measurements in PM67's and PH85's IV curves in the datasheets give the following IV control points:

[i] Current-Voltage
[ii] Advanced Design System
[iii] Output power-Current-Voltage

Table F - 1: PM67's voltage control points and corresponding current levels.

Voltage	**Current**
2 V	2 mA
2.45 V	8 mA

Table F - 2: PH85's voltage control points and corresponding current levels.

Voltage	**Current**
1.6 V	10 mA
1.9 V	30 mA

By DC sweeping and tuning the resistor and DC source in the circuit shown in Figure F - 4, the resistor (Rdiode) and the DC source (V_DC) is selected to match IV-behaviour of the PM67 and PH85. The selected values of Rdiode and V_DC for PM67 and PH85 are shown in Table F - 3.

Table F - 3: Selected resistors and voltage sources for the schematic models.

VCSEL	Rdiode [Ω]	V_DC [V]
PM67	42.8	1.70
PH85	13.0	1.075

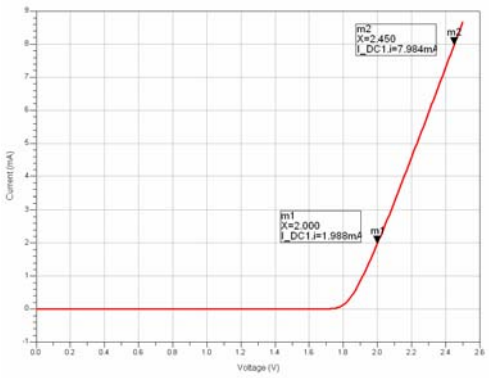

Figure F - 5: DC sweep of the PM67 model.

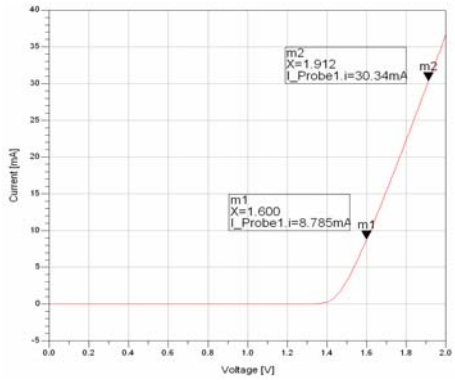

Figure F - 6: DC sweep of the PH85 model.

The two model's IV curves can be seen in Figure F - 5 and Figure F - 6 and the control points comparable to Table F - 1 and Table F - 2, can be seen in Table F - 4 and Table F - 5.

Table F - 4: PM67 model's voltage control points and corresponding current levels.

Voltage	**Current**
2 V	1.988 mA
2.45 V	7.984 mA

Table F - 5: PH85 model's voltage control points and corresponding current levels.

Voltage	**Current**
1.6 V	8.785 mA
1.9 V	~30 mA