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# Development of Electronics for Ultra-Broadband Space Magnetometry

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# Abstract

## Development of Electronics for Ultra-Broadband Space Magnetometry

*Lukas Karlsson*

This master thesis covers various aspects of high frequency, high performance electronics for use with a magnetoresistive magnetometer, realized with micro systems technology, intended for use in space applications, where its small size is essential. The electronic systems for the sensor are designed, built and evaluated during the development phase of the magnetometer, and should consist of amplifier stages, filtering, analog to digital conversion and data acquisition. The report sequentially describes prototype circuit board manufacturing, high frequency layout consideration, component/subsystem selection and different design solutions, based on measurements on designed and manufactured circuit boards. The final results are to be the corner stone of further development of an optimized electronics system, and give the research group a solid base for advanced circuit board manufacturing in future projects.

The work has been done for the Ångström Space Technology Center research group at Uppsala University, Sweden. This final thesis will further be included in a Master of Science Degree in Space Engineering, given at Luleå University of Technology, Sweden.

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TVE 08 004
Sponsor: Rymdstyrelsen, VINNOVA

## Sammanfattning

Detta examensarbebete behandlar design, tillverkning och testning av högfrekvent elektronik, ämnad för att användas tillsammans med en magnetoresistiv magnetfältssensor. Sensorn utvecklas med hjälp av mikrostrukturteknik och har som slutgiltigt mål att vara tillgängligt för rymdindustrin. Elektroniken skall bestå av förstärkare, filter, analog till digital omvandling samt datainsamling på dator. Denna rapport beskriver successivt tillverkningsförfaranden, speciella omständigheter för högfrekvent elektronik, test och utvärdering av komponenter/delsystem samt förslag på design av slutgiltigt system utifrån resultat från körning av tillverkade kretskort och annan hård- och mjukvara. Resultaten tillhandahåller forskargruppen med en robust grund att stå på i den fortsatta utvecklingen av högpresterande elektronik i allmänhet och ett optimerat system för magnetfältssensorn i synnerhet.

Detta arbetet har gjorts för Ångström Rymdtekniskt Centrum vi Uppsala Universitet. Examensarbetet skall i förlängningen inkluderas i en civilingenjörs examen mot rymdteknik, vid LuleåTekniska Universitet.

*To*
*Maria*

# Contents

# Chapter 1

# Introduction

## 1.1 The Ångström Space Technology Center

The *Ångström Space Technology Center* (ÅSTC), is a research group within the Department of Engineering Sciences at the Ångström laboratory at Uppsala University in Sweden. ÅSTC specializes in development of space related technology with MEMS[1] components and systems. The successful projects in the past made it possible for spin-off companies, such as *NanoSpace* and *Ångtröm Aerospace Corporation*, to be established. *Rotundus* and *Kalogi* are also spin-off's from ÅSTC. This spin-off's have enriched Swedish competence and activities in this highly technological space business.

With main funding from the *Swedish National Space Board* and the *Swedish Government Agency for Innovative Systems* (VINNOVA) three project are currently running - SDTM, OCOM and Micropropulsion.The SDTM project aims at developing a miniaturized and high performance magnetometer to be used in space missions with small satellites, *nanosatellites*. This thesis of master degree deals with a set of works related both to general work for ÅSTC and the development of electronics for the SDTM project.

## 1.2 Scope of thesis

The originally intended scope of the thesis, was to develop and test a breadboard electronic set up, to be used together with a magnetic sensor being developed at ÅSTC. The purpose of this was to allow the project to make accurate characterization measurements on the SDTM sensor. During the work, the task has slightly shifted towards process development for making prototype circuit boards. Also, important aspects when working with high bandwidth, sensitive and low noise analog electronics have been included as a theoretical study in the thesis. This theory is extensive, and therefore

[1] Microelectromechanical systems

had to be delimited to the most important aspects and considerations, most relevant to the project.

The work done for the thesis can be divided into two major parts. First, the development part, assisting ÅSTC on improving laboratories, equipment and general manufacturing processes. Second, the electronics, which has been made up of developing electronics for analog signal handling and evaluating different data acquisition methods, including analog to digital conversion. A great amount of time has been spent on finding specific components to be used in the system. The component selection, along with developed designs, described in the subsequent chapters, should be well suited for the project. In combination with the theoretical work and the process development, this report constitute a firm foundation for subsequent work within the project.

In addition to the above, some time has also been spent on studying different magnetometry solutions used in space applications today, and contributing, where possible, to the compilation of the requirements specification document for the project. This is described in more detail later in the following chapter.

# Chapter 2

# Background

## 2.1 Magnetic field sensors and magnetoresistance

Today there is a number of different kinds of magnetometers used in space applications [3]. They are used for various tasks, such as orbital/attitude control and for sensing the magnetic field in the study of its properties and important plasma phenomena in our solar system. The most commonly used are the fluxgate, search coil and superconductive quantum interface magnetometers. Others are hall effect, proton precession and optically pumped magnetometers.

The fluxgate magnetometer has two coils surrounding a common magnetic core. By driving one of the coils with a current the core is magnetized. By measuring the demagnetization of this coil with the other one, the ambient magnetic filed can be deduced. The main advantage of the fluxgate is its simplicity and low cost. The major drawback is that the size of the sensor must be fairly large to keep noise down. Fluxgates have relatively low in bandwidth, and the sensitivity usually depends on the geometry and size of the sensor.

The search coil magnetometer uses only one coil around a core with high permeability. The external magnetic field is related to a small but measurable current in the coil. The bandwidth of this sensor is higher than for the fluxgate, but still limited. It has the same drawback as the fluxgate considering noise and size.

One of the most sensitive magnetometers[1] used today is the superconductive quantum interface magnetometer (SQUID). The sensor is basically a superconductive closed loop that responds to a magnetic flux through it with a current that satisfies the requirement of flux quantization in superconductors. SQUIDs only operate at very low temperatures, just a few Kelvin, and are therefore a bad choice for space applications where temperature regulation often is a problem. Even so, the exceptional performance of the

[1] 2007-09-02 http://www.ias.ac.in/currsci/sep25/articles17.htm

sensor makes it very useful in non-space applications where cooling is less of a problem.

The Hall effect sensor uses the fact that moving charged particles in a conductor experience the Lorentz force when subjected to an external magnetic field. The result is that the charge density in the conductor will vary according to the external field. The Hall effect sensor measures these variations to acquire the magnetic field. The sensor usually has quite a low sensitivity but can be improved by using ferromagnetic conductors.

The proton precession magnetometer measures the time varying precession of polarized hydrogen atoms when under the influence of an external magnetic field. The frequency of the precession is know from quantum mechanics as the Larmor frequency and can be measured very accurately. The sensor is reliable and inexpensive, but suffers from problems when measuring fields that vary much in time and space.

Optically pumped magnetometers use the absorbtion and emission of photons in a gas to measure magnetic fields. When the gas absorbs a photon it excites an atom which then decays back to its original state. In the absence of a magnetic field, the decay reemits a photon that is equal to the one absorbed. If an external field is applied to the gas, electrons will precede around the field lines with the Larmor frequency. The decaying electrons will then polarize their emission. The magnitude of the external magnetic field can then be deduced by measuring the difference in polarization of the incoming and outgoing light.

There is an increasing demand for magnetic sensors with high sensitivity, small size and high bandwidth. A promising technology in the field of efficient and miniaturized magnetic sensors is magnetoresistance. The principle is to use a material or combination of materials which vary their resistance when placed in a magnetic field. There are four types of such elements, namely Giant Magnetoresistance (GMR), Magnetic Tunnel Junctions (MTJ), Anisotropic Magnetoresistance (AMR) and Spin Valves (SV). These are all based on the fact that the polarization of a material caused by an external magnetic field alters the conductivity of a ferromagnetic material.

The simplest type is the AMR. It has a single strip of a ferromagnetic conductor. Along the strip there is a constant bias voltage. The highest conductivity is when the polarization of the electrons in the conductor is aligned parallel with the applied voltage. The lowest conductivity, i.e. the highest resistance is when the electrons are aligned perpendicular to the voltage. By monitoring the variations in the voltage over the sensor the magnitude of the external field is found with respect to the orientation of the sensor.

The SV sensor has two ferromagnetic layers separated by a non-magnetic conductor. One of the layers act as a reference layer with a certain fixed spin polarization, whereas the other is a sensing layer that changes its polariza-

tion according to an externally applied magnetic field. When a voltage is applied perpendicular to the layers, the magnetoresistance of the sensor depends on the polarization of the sensing ferromagnetic layer. If it is parallel to the reference layer, current can flow more easily, while an antiparallel polarization will make it more difficult for electrons to pass from one layer into the other. The current is then measured and considered proportional to the external magnetic field.

Magnetic tunneling junctions, MTJ:s, are very similar to spin valves. The main difference is that the MTJ uses a dielectric layer as a barrier instead of the non-magnetic conductor. The barrier needs to be very thin, so that electrons from one layer can tunnel through the barrier, thus creating a current in the device. Since the electrons have a spin their orientation will align with the external magnetic field. The reference layer will prefer electrons with the same spin orientation as the ones already in the polarized material. The amount of tunneling electrons through the barrier should be directly proportional to the spin orientation of the sensing layer, and by this the orientation of the externally applied magnetic field.

A review study of magnetic sensors [3] conducted in the early phase of this project pointed out that a MEMS-tailored sensor of the MTJ type should be the best choice.

## 2.2 Conceptual presentation of the SDTM sensor

SDTM is short for *Spin dependent tunneling magnetometer*. The understanding of the basic theory for the SDTM sensor is of great importance when designing interfacing electronics for the sensor. This section is mainly in reference to the WP4 report for the SDTM [1]. The SDTM sensor is based on the concepts and physics of magnetic tunneling junctions described above. The layer configuration is shown in Figure 2.1, where many MTJ's are configured in parallel. The barrier material of the SDTM will be $Al_2O_3$. This material offers high magnetoresistance, especially when combined with the CoFe-CoFeZr electrodes. High magnetoresistance in combination with low noise and hysteresis are key elements in the choice of materials and configurations.

The elementary arrangement of the SDTM sensor can be divided into three levels: The first level is the individual sensor elements, which consist of many MTJ elements connected in parallel to maximize performance and minimizing SNR[2]. This is illustrated in Figure 2.1. The second level is the set up of the basic sensing device. The individual sensor elements are connected in series to increase resistance, and thus the signal output. These devices are then configured as a Wheatstone bridge, utilizing four of them to form a balanced differential output. The Wheatstone configuration is illustrated in

[2]Signal to noise ratio

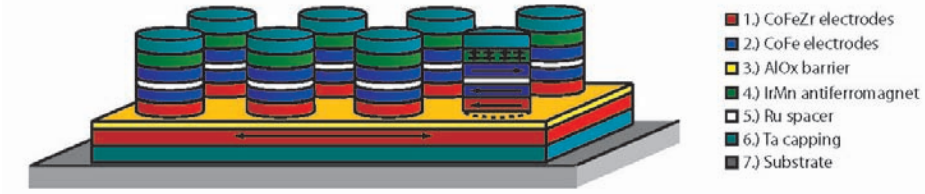


Figure 2.1: Paralleling of many layer elements.

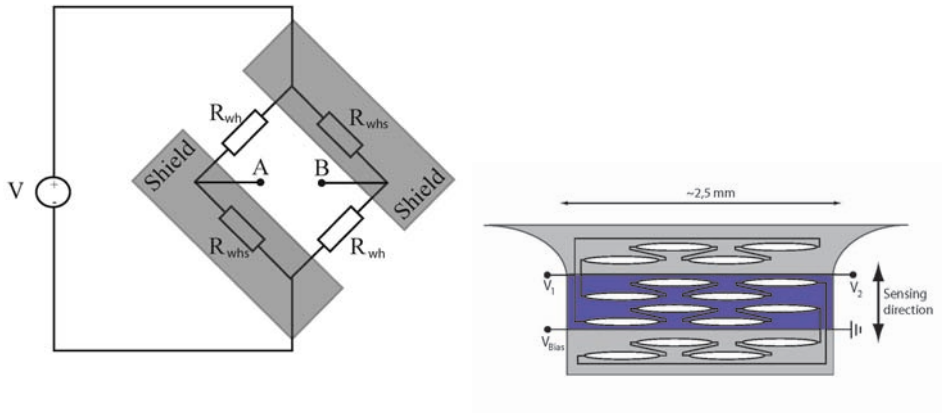


Figure 2.2: The Wheatstone configuration. To the left the electronic schematic (left) and the actual physical layout with the unshielded elements in the center (right).

Figure 2.2. As shown in the figure, two of the sensing devices are shielded and so act as reference in each half of the bridge. The other two are not shielded and therefore change their resistance with an externally applied magnetic field. The resistance, $R_{wh}$ of a non-shielded device can be described by:

$$R_{wh} = \frac{M}{N}(R_0 + \Delta R), \tag{2.1}$$

where $M$ is the number of sensor elements connected in series and $N$ the number of MTJ's in parallel. $R_0$ is the resistance when no external field is present and $\Delta R$ the change in resistance due to the magnetic field for each MTJ. The shielded devices have $\Delta R = 0$ and their resistance $R_{whs}$ given by:

$$R_{whs} = \frac{MR_0}{N}. \tag{2.2}$$

As seen in Figure 2.2 the output from the Wheatstone bridge is taken as the voltage between nodes A and B. The shielded and unshielded devices acts as voltage dividers with a differential balanced output centered around $V_{bias}/2$. Using voltage division and inserting Equations 2.1 and 2.2, the differential output voltage becomes:

$$V_A - V_B = \frac{R_{wh}}{R_{wh} + R_{whs}}V_{bias} - \frac{R_{whs}}{R_{wh} + R_{whs}}V_{bias} = \frac{\Delta R}{2R_0 + \Delta R}V_{bias}. \tag{2.3}$$

The benefits of using the Wheatstone bridge is that the signal is always taken differentially, independent of the common mode level. In addition to an increase in signal strength, this also means that the output signal is zero when there is no applied magnetic field to the sensor. The configuration also allows lower bias voltages, resulting in less noise and, by this, higher sensitivity. Temperature stability is also a key factor in the decision of using the Wheatstone.

Each Wheatstone bridge can provide the magnitude of the external field in relation to a symmetry axis. To get a two-dimensional representation of the field more than one bridge needs to be used, the simplest case then being to use two Wheatstone sensors in a 90° orientation. The SDTM in this project employs yet another solution by configuring three Wheatstone sensors 120° apart, Figure 2.3. This is the third level of the SDTM sensor set up. This rosette configuration ensures that there is always a non-zero signal on at least two individual Wheatstone sensors, thus further limiting noise, and increasing the range and sensitivity of the sensor. The rosette configuration also includes a calibration coil, used for resetting the all sensors by saturating them. These coils are also shown in Figure 2.3 as conductors going through all three sensors.

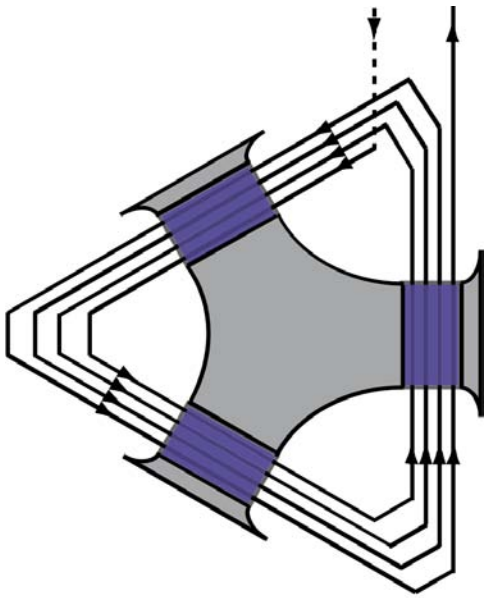

Figure 2.3: 120° rosette configuration of Wheatstone sensors. Also showing calibration coil setup used for sensor reset.

Three-dimensional measurements are enabled by using two rosettes set up perpendicular to each other. A more thorough description of the SDTM can be found in [1] and [3].

The SDTM has at least two potential applications, one being as a highly sensitive broadband magnetometer for making 3-D measurements of magnetic fields in space, the second to operate it as a broadband antenna for picking up magnetic field transmissions of relatively weak power. The latter is highly interesting in many areas and could be a major application once investigated further. Miniaturized magnetometers are also required in many high-end technologies used today, such as the car industry and aerospace technology.

## 2.3 Requirements specification

The requirements specification document, is where goals and guidelines concerning a specific mission for the project are defined. For the SDTM, being a new type of sensor, there is no specific mission to base the requirements on. So, for the document to be created, a fictive mission had to be created [2]. To decide this fictive mission several important missions were studied and compared. The most demanding requirements found in several categories were then used as a base for setting the SDTM requirements. The requirements set for SDTM and their origins are found in Table 2.1.

Table 2.1: Requirements specification for SDTM with source of origin.

| Origin | Requirement | Value | Unit |
|---|---|---|---|
| Cassini | Noise at 1 Hz | 3.9 | $pT/\sqrt{Hz}$ |
| Rosetta | Noise at 10 Hz | 14 | $pT/\sqrt{Hz}$ |
| Themis | Resolution | 3 | $pT$ |
| Cluster | Field range | 65 | $\mu T$ |
| OAM (fictive) | Bandwidth | 500 | $MHz$ |
| N/A | Mass | 0.02 | $kg$ |
| N/A | Power consumption | 1 | $W$ |
| Venus Express | Temperature range | -160/120 | $^{\circ}C$ |
| Galileo | Radiation dose | 150 | $krad$ |

When looking for these requirements many missions were studied. Among them Rosetta, Cassini, Galileo, Venus Express, Cluster and Themis. A summary of these missions and their magnetic instruments, along with specific requirements for the sensors and spacecrafts are found in Appendix A.

# Chapter 3

# Development of Manufacturing Processes

Although not originally intended, the work of finding and evaluating processes for making prototype circuit boards became a major part of the thesis. Most of the processes follow standard procedures in electronics, but some have been developed to suit the capabilities of ÅSTC. At the beginning of the work, basic skills in circuit board layout software were established, followed by learning and applying rules to mill out circuit boards from copper laminates and finally manufacturing the circuit boards by mounting components and do the solder work. Much time has been spent to find suitable processes and techniques for manufacturing good quality circuit boards for the SDTM project, find and acquire new equipment and components, and organize them. The *Institute of Space Physics, IRF*, offered access to their laboratory and equipment. Knowledge and experience of working with high speed electronics was also available at IRF.

The remain of this chapter describes the so called infrastructure work, which has become an important part of the thesis. This is essential work to provide functional facilities for electronic development, required for both this thesis and other projects carried out in the research group. Appendices B and C include two tutorials for developing circuits boards, both written as a part of the thesis.

## 3.1 Software

The software used for designing electronics was "Advanced Design System" (ADS) from Agilent Technologies. This software suit is mainly written for microwave electronic engineering, but can also very efficiently be used for designing standard circuit boards and for simulations. Although no previous experience in ADS was present at the start of the thesis, a few weeks was enough to master the various parts of the software for designing circuits and

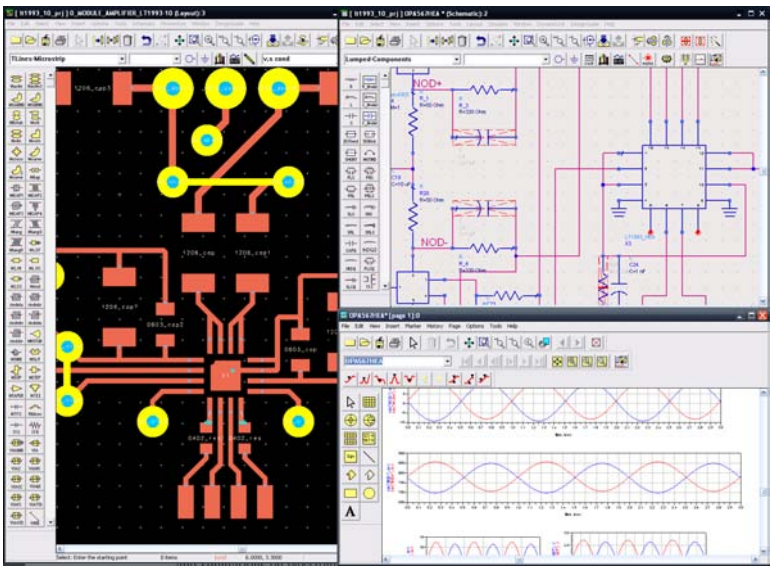

Figure 3.1: A typical screen when using Advanced Design System, showing layout, schematic and simulation windows.

setting up basic simulations.

The ADS software suit is made up of three major parts: *Schematic*, *Simulation* and *Layout*, Figure 3.1. The circuit schematics plays a central role in the work of making circuit boards, and it is the reference for both the simulation and the layout software. Here, models (usually *SPICE*) of many fundamental circuits can be imported. These models can be used to make a certain circuit, which then can be simulated in either the time domain or the frequency domain. The whole circuit can then be imported element by element into the circuit layout software where the circuit board is designed. When designing circuit boards there are many things to consider, such as issues relating to how to place components and route the wires between them. Some of these considerations are further described in Chapter 4, along with some other important electronic theory.

## 3.2 Milling

After having a complete layout for a circuit board there are several ways to manufacture these. Etching, printing and milling are the methods usually giving the most reliable results as they can house surface mounted components. Equipment for etching was not available during the work and ordering printed circuit boards is very expensive, especially when the behavior of the electronics is not fully predictable. IRF had just recently acquired the


Figure 3.2: ProtoMat S62 circuit board plotter. (image taken from LPKF AG webpage www.lpkf.com).

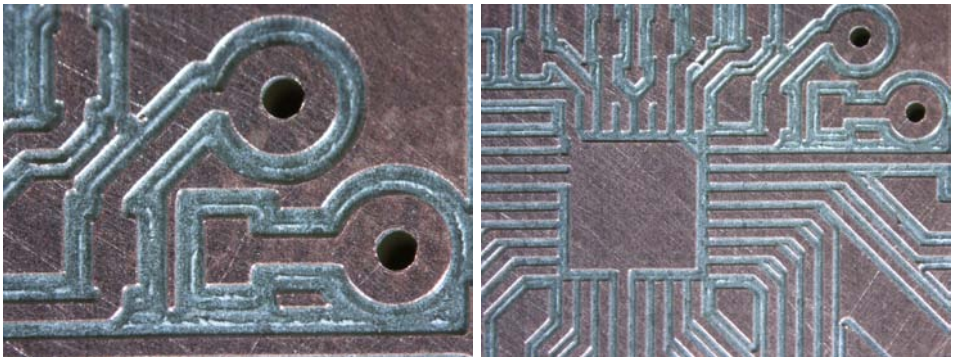

Figure 3.3: Circuit boards milled out with the S62 circuit board plotter from LPKF. Traces are 0.25 mm wide.

ProtoMat S62 circuit board plotter from *LPKF Laser & Electronics AG*[1], Figure 3.2, that rapidly can mill out circuit boards. The plotter uses the information from *Gerber* and *NC/Excellon* files, exported from ADS, to drill and mill two layer circuit boards. The main used tool for milling was a 0.2 mm universal cutter with a conical shape that contours clearance in the copper layer from traces, component footprints and other geometrical shapes included in the CAD drawing. Besides the universal cutter, many other tools were also used, such as drills, cutters and larger milling tools.

[1] http://www.lpkf.com/products/rapid-pcb-prototyping/circuit-board-plotter/protomat-s62/index.htm

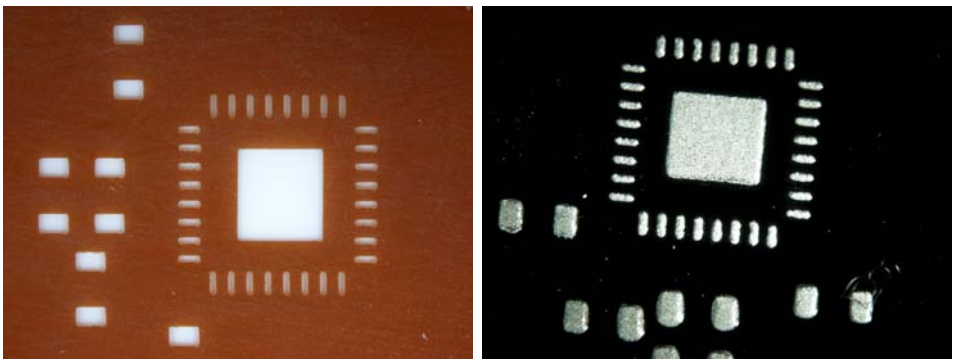

Figure 3.4: Example of a Kapton screen mask for solder paste printing to the left and a typical screening result to the right. Pads are 0.25 mm wide.

## 3.3 Solder paste screen printing

As many high performance components are surface mounted and usually have very small pad sizes, the use of solder paste screen printing is required for making good solder work. A solder screen mask has small openings to define the where the solder paste should be. The thickness of the screen mask, along with the opening sizes determines the amount of paste being left on the board after screen printing. Screen masks made of stainless steel or plastic foils can be ordered from companies such as *HP Etch*[2], or electronic circuit board manufacturers, where they are usually cut out by etching, high precision laser or water jet cutters. These screen masks are of high quality and outstanding precision, but are very expensive, unless a large quantity is ordered. Small series or, as here, prototyping seldom justify this cost. Since the circuit board plotter was available at IRF the idea of using it to cut out screens was born. To do this a thin, tough, reliable and heat tolerant material had to be used. Kapton film meets these requirements and was therefore tried out. At first the same universal cutter (0.2 mm) used for making circuit boards was employed, with poor result due to the conical shape of the tool. However, a straight HF mill with a diameter of 0.15 mm dramatically improved the results, Figure 3.4.

## 3.4 Placing components

When the solder paste has been screen printed on the circuit boards the components are carefully aligned and placed on their positions. Surface mounted components (SMT:s) are small, light and require precise placement to avoid bad solder work when heated. This can usually not be made by hand, so a vacuum powered *pick-and-place* equipment and a microscope was

[2]http://www.hpetch.se

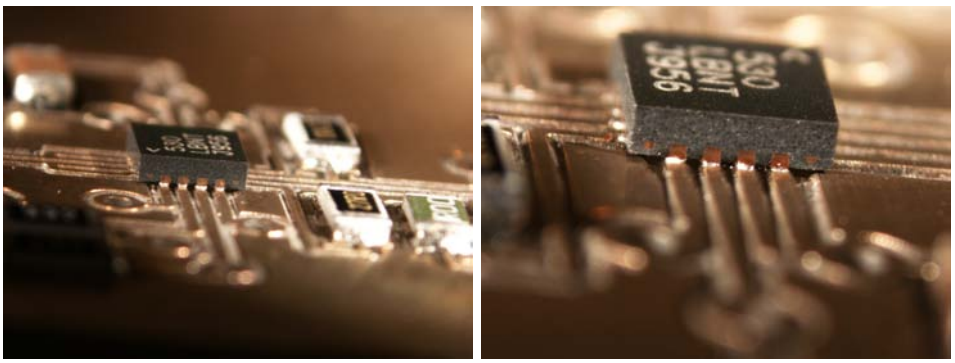

Figure 3.5: Perfectly soldered QFN package with pads located underneath. Package is 3 x 3 mm large

used for this work. With the help of vacuum, a tiny needle holds a single component until it is released on its designated position on the circuit board.

## 3.5 Soldering

Smaller component should, when building high performance electronics, be soldered through reflow soldering, usually in a designated oven, while larger components, such as coaxial connectors and pin-through vias, can be done by hand soldering. The ÅSTC laboratory does not have a good enough oven, so improvisation was the way to solve the problem. The use of a heated plate was established as the method for reflow soldering. There are, in fact, advantages of using this method. For instance, it is easier to monitor the soldering process and verify its completion. Also, heat is concentrated to the board itself, thus preventing components from being overheated and still allow the ability to closely follow reflow profiles given in component data sheets.

# Chapter 4

# Important Aspects for High Speed Electronics

The design of broadband and high frequency circuit boards presents the designer with numerous problems, such as electromagnetic interference, grounding and parasitic components. Careful layout work using some rules and a lot of advice may mitigate the problems. Yet, trial and error processes are often required to obtain the best results. The following sections will briefly introduce the most important of these issues.

## 4.1 Grounding

Proper grounding is probably the most important aspect when working with high frequency electronics. Ground planes not only act as a common reference voltage to the entire circuit, but also provide a low impedance trace for returning currents to follow. One-layer circuit boards with routed ground traces usually lead to problems at high frequencies. When doing high frequency designs, one usually uses a ground plane that completely covers at least one plane in multilayer circuit boards. If a two layered board is used, the bottom layer is usually the ground plane, and all connections, routing and components are placed in the top layer. This allows the currents to follow the lowest impedance path back to the source. The lowest impedance return path for DC is simply the path of lowest resistance, while for high frequencies, inductances and capacitances add to the total impedance. The return current at high frequencies can therefore be rather complicated to predict. An unbroken ground plane lets the current find the most efficient trace back on its own, this means that it will travel back as close to the outgoing current as possible. An example of a proper and clean ground plane, designed here, is found in Figure 4.1(left).

When working with both analog and digital circuitry on the same board it is important to place the digital and analog components in separate region

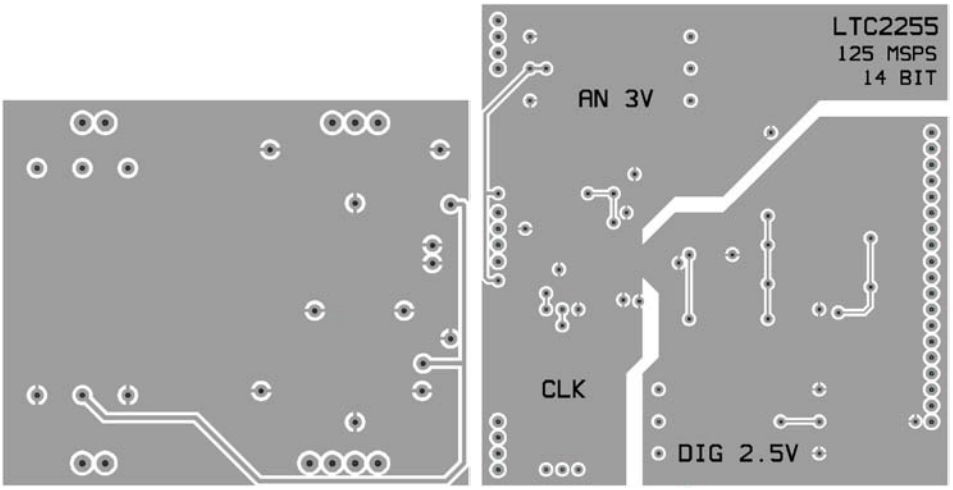


Figure 4.1: Examples of techniques when designing ground planes: Proper unbroken ground plane (left). Split ground plane for circuit board containing both analog and digital components (right).

to minimize ground plane interference. The fast rising edges in digital signals create current spikes in the ground plane, which can interfere severely with sensitive analog devices. As a precaution the ground plane can also be broken between the digital and analog part of a circuit board, only connecting them at a narrow bridge - preferably underneath some component that includes both analog and digital parts, such as an AD-converter. This is to prevent excess currents to circle on either of the ground plane, and still set a common reference voltage for the whole board. An example of a split ground plane is found in Figure 4.1(right).

Another important aspect of using ground planes is to limit the effect of parasitic capacitances and inductances. Parasitics exist independent of frequency, but even small ones are clearly noticeable at higher frequencies when the impedance changes. Many parts of a circuit board can give raise to these parasitics, such as long traces, component pads, vias and some discrete components. Figure 4.2 illustrates a non-inverting operational amplifier design with and without parasitics.

Capacitances in combination with inductances can form resonant circuits with extensive peaking at high frequencies. This can be limited by using a proper ground plane to minimize inductances due to looping return currents. Figure 4.3 shows the effects of peaking and oscillations due to parasitics on circuit boards. The stray capacitances usually arise from parallel plates, such as pads, in the design and can also be limited by smart design solutions. One of the more important contributors to parasitics are vias that connect one layer of a circuit board to another. The inductance and capacitance of vias can be calculated with Equations 4.1 and 4.2, where $d$ is the drill hole

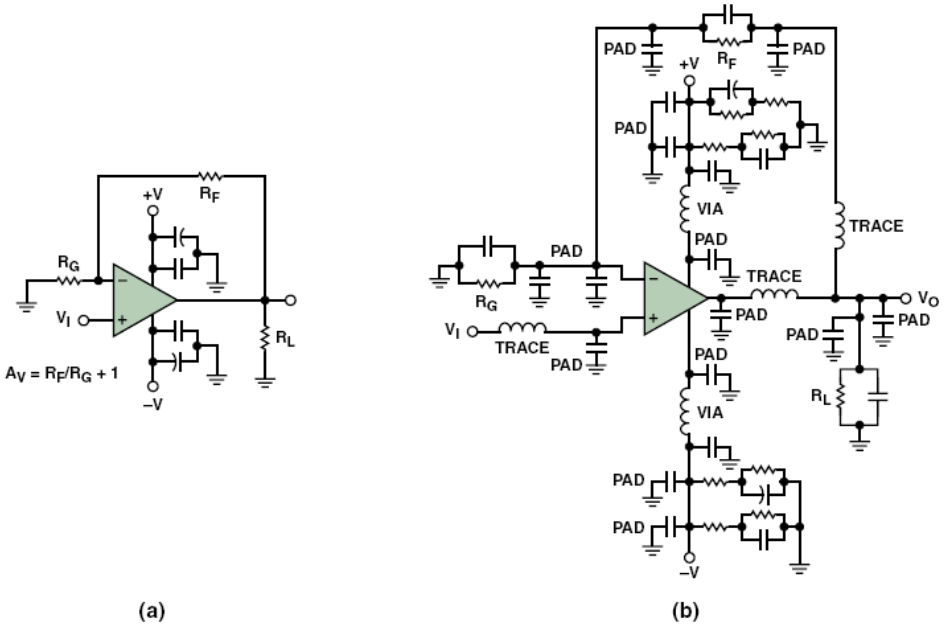


Figure 4.2: Illustration of the circuit complexity when taking the influence of parasitics into account in a simple circuit design [4].

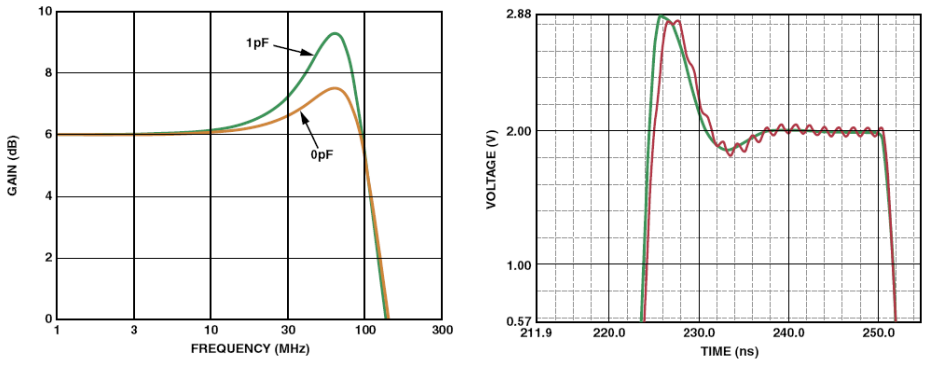


Figure 4.3: Left: Parasitic capacitances cause peaking at high frequencies. Right: A proper ground plane can mitigate oscillation problems caused by parasitic inductance [4].

diameter, $D1$ the conductive pad size around the hole, $D2$ the clearance to the ground plane, $T$ the board thickness and $\epsilon_r$ the relative permeability of the board material.

$$C = \frac{0.55\epsilon_r T D_1}{D_2 - D_1} \quad pF. \tag{4.1}$$

$$L = 2T\Big(\ln\frac{4T}{d} + 1\Big) \quad nH. \tag{4.2}$$

The influence from vias can be limited by using small plated vias or make the layout using the least possible number of vias.

## 4.2 Decoupling and bypassing

High frequency analog electronics are very sensitive to noise present at the supply lines. These must therefore be properly bypassed with capacitors to ground. Usually at least two different capacitors of different size are used. This is to make the supply "see" a low impedance over a wide range of frequencies - as seen in Figure 4.4. If the supply current to the device is known to be low, a low value series resistor can be added between the bypass capacitors and the supply pin of the component. This further dampens the high frequency noise present at the bypass by creating a low pass RC network. Decoupling is a more general term for bypass capacitors and applies to all situation where one part of a circuit is bypassed to another part with a capacitance. Decoupling can, for example, be used between two differential signal traces, that in combination with resistances create a differential low pass filter. The term bypassing normally reefers to the decoupling of a supply to ground or another supply.

When working with really high frequencies, around RF and above, decoupling becomes more complex. This is because one has to consider the effects from the parasitic as well as inductance present in all capacitors. These effects create a lot of small LC resonant circuits that have to be considered when designing bypass networks. Usually, designers use the capacitances between power and ground planes, and other parasitics to work in their favor.

## 4.3 Noise

In amplifier designs, the definition of noise is a signal present at the output that cannot be traced back to the amplifier inputs. There can be many sources of noise, and to eliminate them entirely is impossible. Noise is conventionally divided into different colors as shown in Table 4.1. These colors are set to correspond to the frequency dependance of the noise, in a similar

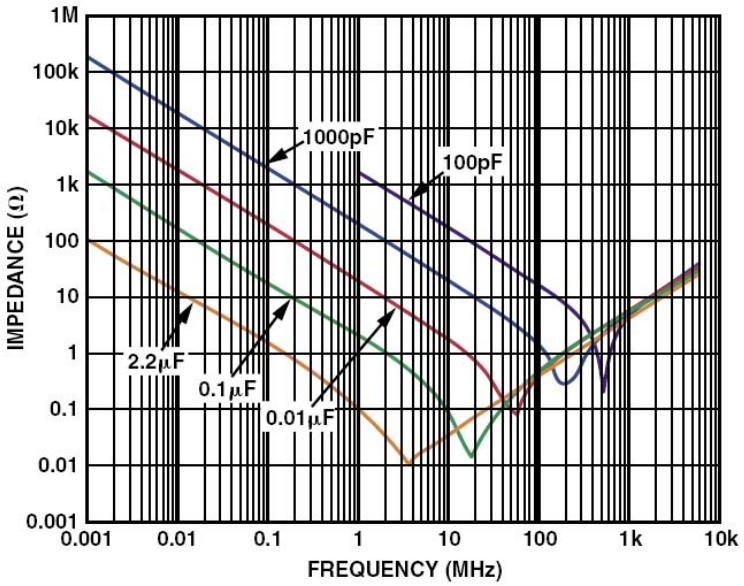


Figure 4.4: The impedance of capacitors of different values varies with frequency [4].

Table 4.1: Noise colors and their frequency content [5].

| Color | Frequency content |
|---|---|
| Purple | $f^2$ |
| Blue | $f$ |
| White | 1 |
| Pink | $1/f$ |
| Red/Brown | $1/f^2$ |

way as visible light is. Most electronics have a dominating noise spectrum in the white and pink region.

The noise in an amplifier is usually given in units of $nV/\sqrt{Hz}$. What this means is that the total noise at the output of the amplifier increases with the bandwidth. A common noise figure for a high performance op-amp can be 2 $nV/\sqrt{Hz}$. Thus, if the bandwidth of this amplifier is 600 MHz, the total noise becomes 49 $\mu V$. This is unacceptable in many applications where high resolution is required, for example when pre-amplifying a signal for AD-conversion.

One of the most common sources of noise is thermal noise, $E_{th}$, described by:

$$E_{th} = \sqrt{4kTRB}, \tag{4.3}$$

where $k$ is Boltzmann's constant, $T$ the temperature in Kelvin, $R$ the resistance, and $B$ the noise bandwidth [5]. So, by lowering the working temperature we can lower the noise in the resistor, but a far easier way is to use lower valued resistors or limit the bandwidth. Cutting down on bandwidth in favor of less noise i a typical trade off frequently encountered when working with electronics.

Shot noise is the result of quantum effects where conductive electrons suddenly change their energy to kinetic when they breach a potential barrier, for example a transistor PN junction [5]. This means that the total power of shot noise depends on the total current flowing.

Both shot and thermal noise are approximately white noise, so they do not depend on frequency. Although, they do depend on the total bandwidth. Therefore they can easily become the dominant noise source in high bandwidth applications. At low frequencies pink, or 1/f, noise is dominant and there is usually no way to limit this considerably.

The noise floor is defined as the level of noise present at the output of an amplifier when all input sources are turned off [5]. This noise determines the smallest signal possible for which the amplifier is useful. This is something that has do be determined for each design through testing.

## 4.4 Impedance and matching

Impedance matching refers to the techniques used to make a source impedance equal a load impedance to maximize the energy transfer between these. The simplest case of this is shown in Figure 4.5 where source, transmission line and load impedances are considered. The energy not put through the load is instead reflected back to the source, due to a mismatch of two impedances. One method of doing this is to use the complex conjugate of the two impedances, where the real part is the resistance and the imaginary part the reactance. This means that matching is achieved if the the source and load reactance are equal in magnitude but of opposite sign. Reactance arises from reactive components, such as capacitors and inductors. The electrical length compared to the wavelength is also of interest. A rule of thumb is that if the wavelength is more than four times the electrical length, impedance matching is of no importance. In that case the waveform can be approximated as constant over the electrical length and so reflections are irrelevant.

## 4.5 EMI and EMC

EMI, *Electromagnetic Interference*, is interference caused by a source and detected by a susceptible victim via a coupling path [7]. The interference will

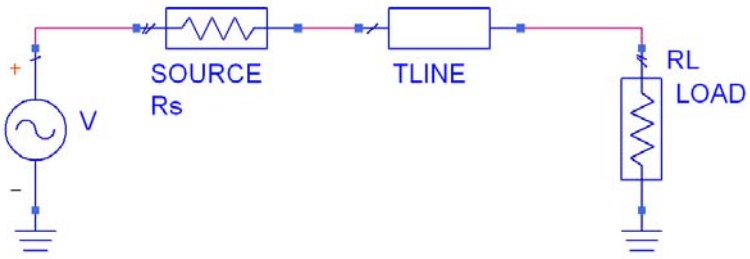


Figure 4.5: A very simple example of impedance network, where source, load and transmission line impedances must be matched to provide maximum power transfer onto the load.

inherently affect the performance of most electronic devices and is a major concern when designing high frequency circuit boards. EMC, *Electromagnetic Compatibility*, is the ability of electronic systems to function properly in an environment without causing or accepting EMI above a certain level. All system designs should be tested to match the proper EMC requirements. The coupling of EMI can have one of the following mechanisms [7]:

1. Conduction - electric current
2. Radiation - electromagnetic field
3. Capacitive Coupling - electric field
4. Inductive Coupling - magnetic field

According to Maxwell's equations, a time-varying electric or magnetic field will give rise to a change in the other. On circuit boards there are many currents and potentials that will have fast changes in time, especially when dealing with high frequencies. These will then create time-varying electromagnetic fields that can affect other parts of the circuit board or any other nearby electronic device. Therefore, it is important to limit the ability of the circuit board to radiate these fields. The most common reason are current loops that occur when return currents have to take a different way than the outward current does. Also, routing is important to avoid traces to act as transmission lines or radiators (antennas). Even at lengths as short as one twentieth of a wavelength, a circuit board trace can become an efficient antenna [8].

When a trace have high running currents, inductive coupling causes crosstalk between traces that run parallel and close to each other. Because of this, sensitive signal traces should not run parallel to other traces that have high coupling effects. At low currents the effect is instead capacitive due to potential differences between traces with similar problems. This can be limited by decreasing the seen capacitance between traces.

When using balanced differential signal traces, EMC is greatly improved. Radiation is limited due to the equal and opposite nature of differential signals, where they cancel each other out. As victims differential pairs are also very good since both traces will be equally perturbed and so only a common mode shift will occur [9].

Usually the same mechanisms that cause EMI, are also susceptible to pick up interference. The rules of EMC therefore apply equally to limitation of emission and pick up of interference.

## 4.6 Materials

Although not as important as the other aspects to circuit board theory, the composition and making of circuit boards play a rolel [18]. The thickness of the board as well as the dielectric material is important for capacitive effects, as shown in Equation 4.1. The dielectric could, if exposed to a potential difference of several kV also break down and short-circuit two layers of the circuit board. The thickness of the dielectric spacer is also affected by the ambient temperature, especially if it reaches the glass transition temperature, when the thickness can vary with several percent. Most manufacturers offer circuit boards especially made for housing high speed electronics.

# Chapter 5

# SDTM Electronic Theory, Components and Systems

The basic electronics for interfacing and collecting data from the SDTM sensor is not an advanced design, as seen in the block scheme in Figure 5.1. Although the high frequencies and high performance electronics, which are used to fulfill the requirements specification, have been the source of many problems and nearly endless efforts for trouble shooting. This chapter will describe the functionality and some important aspects to each block in Figure 5.1, and take a deeper look into the more important components, concepts and theory that has been chosen to realize the tasks at hand.

## 5.1 Magnetic sensor

As a substitute for the real SDTM sensor, a similar sensor from *NVE Corporation* has been used for this thesis. This *AAL002-02* sensor utilizes a Wheatstone configuration and GMR, *Giant Magnetoresistance*. Thus, making it similar enough to the SDTM to be used as a replacement. The Wheatstone bridge configuration is a very strong solution in sensing applications. The output from the bridge is a balanced differential signal, meaning that there will be zero signal at zero magnetic field. A balanced differential signal also means that the two output voltages from the sensor will be of equal magnitude, but of opposite sign or 180° out of phase at all time. Thus, the common voltage noise from the sensor will be much less significant. The differential output voltage from a Wheatstone bridge, as derived in Chapter 2, is:

$$V_A - V_B = \frac{\Delta R}{2R_0 + \Delta R} V_{bias}, \tag{5.1}$$

where $\Delta R$ is the change in resistance due to a magnetic field, or simply the

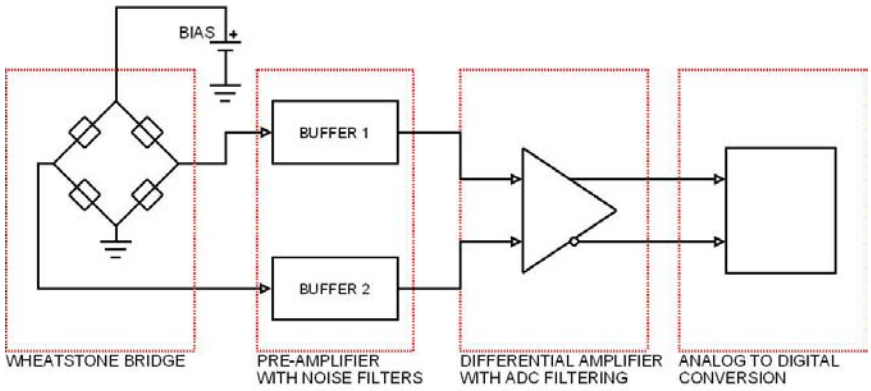


Figure 5.1: Low level block scheme of the basic electronics needed for interfacing the SDTM sensor.

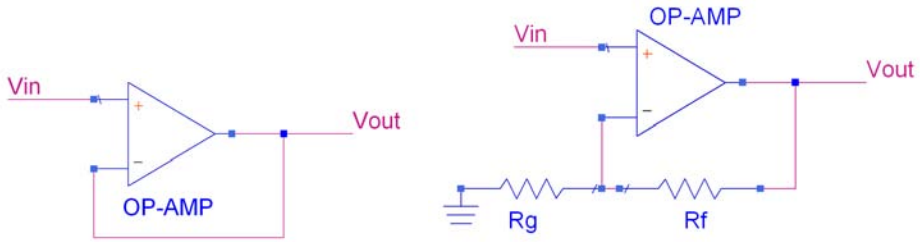


Figure 5.2: To the left: non-inverting voltage follower or buffer. To the right: non-inverting buffered gain block.

*magnetoresistance*, and $R_0$ is the resistance when no field is applied. For the AAL002 sensor $R_0$ is approximately 5.5 k$\Omega$ and $\Delta R$ is as high as $\pm 20\%$ [11].

## 5.2 Pre-Amplifier, Buffer

The purpose of the pre-amplifier is to *buffer* the differential signal coming from the Wheatstone sensor. Buffering means that the signal is isolated from the subsequent output/differential amplifier by utilizing a high impedance input immediately after the sensor. The buffering limits the leakage currents from the sensor, which, in the case of a low impedance amplifier, can be extensive. Buffering also greatly simplifies the impedance matching, as the input in most cases can be considered infinite impedance.

A buffer stage uses operational amplifiers set up in a non-inverting configuration, as seen in Figure 5.2. The design can either be a voltage follower with no feedback resistor where the output voltage is equal to the input voltage, or as a gain block circuit where the output voltage, $V_{out}$ is given by [12]:

$$v_{out} = v_{in} + \frac{v_{in}}{R_g} R_f = v_{in}\Big(1 + \frac{R_f}{R_g}\Big), \tag{5.2}$$

where $R_f$ and $R_g$ are feedback and gain resistor values, as shown in Figure 5.2. High frequency operational amplifiers, usually require a certain minimum gain to remain in a stable state. Therefore the voltage follower is not a suitable design for these requirements to be fulfilled. Instead high speed buffer stages are configured with a gain. Usually a major part of the amplifier chain gain is given from the buffer pre-amplifiers.

In the case of a differential buffer/pre-amplifier, two amplifiers have to be used, one for each differential signal path. For this, it is very important that the configuration doesn't disrupt the balanced behavior of the signal. This requires both amplifiers to be configured as equally as possible, as any difference in resistor values will cause extensive loss in CMRR[1] and resulting distortion of the signal. The common mode problem is easily handled by connection the two amplifiers over a shared gain resistor $R_g$, as seen in the left schematic in Figure reffig:inamps. This will force the two amplifiers to always have the same current in each feedback loop, and thus minimizes any matching errors. It also result in zero common mode current, thus increasing the common mode rejection greatly. This configuration is the input stage of a classic *Instrumentation Amplifier*. If the differential input voltage, $V_{id}$, is given by $V_{i2} - V_{i1}$, where $V_{i1}$ and $V_{i2}$ are the individual input voltages, and the differential output voltage, $V_{od}$ equivalently is given by $V_{o2} - V_{o1}$, we get:

$$V_{od} = V_{o2} - V_{o1} = V_{i2} + \frac{V_{id}}{Rg} R_f - \Big(V_{i1} - \frac{V_{id}}{R_g} R_f\Big) \Rightarrow \tag{5.3}$$

$$\Rightarrow V_{od} = V_{i2} - V_{i1} + \frac{V_{id}}{R_g} R_f + \frac{V_{id}}{R_g} R_f = \Big(1 + \frac{2R_f}{R_g}\Big) V_{id}. \tag{5.4}$$

Although this is good enough in most cases it is not suitable when interfacing components that cannot handle negative voltages. The subsequent differential amplifiers described in Section 5.3 almost always utilize single power supply. Since the above described buffers stages have a non-zero gain, their outputs will swing in large amplitude around the input common mode set by the common mode voltage of the Wheatstone bridge. Since the Wheatstone bridges of the SDTM and AAL002 sensors are biased at low voltages to minimize noise, the buffer output will swing to negative voltages due to the gain. This cannot be handled by the single-supply differential amplifier. Therefore the common mode voltage at the output of the buffers must be level shifted upwards, so that there will only be positive voltage swings present at the output. The level shifting also decreases distortion as the

[1] Common Mode Rejection Ratio

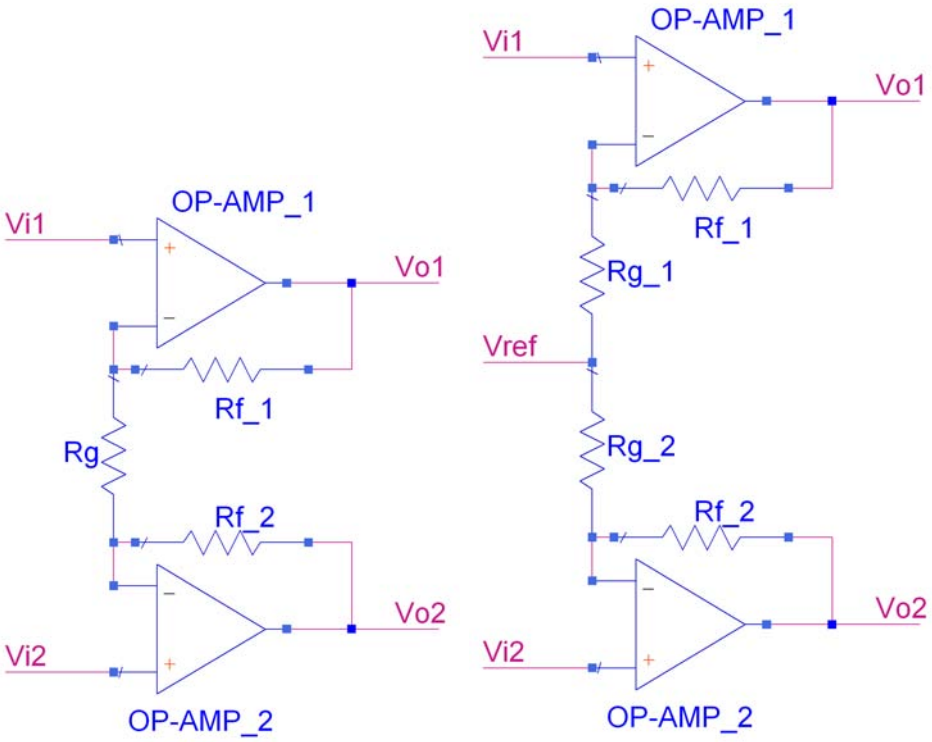


Figure 5.3: Differential buffer amplifier input stages, one normal and one with output common mode shift using a reference voltage.

signal amplitude gets further away from the supply, and should also lower noise figures. Shifting can be done by introducing a reference voltage in the circuit, by splitting the gain resistor $R_g$ into two equal resistors and connecting a negative reference between them, as in Figure 5.3. With the reference included, the output voltage of a single buffer amplifier becomes [15]:

$$V_{o1} = V_{i1}\Big(1 + \frac{R_f}{R_g}\Big) - V_{ref}\frac{R_f}{R_g}, \tag{5.5}$$

$$V_{o2} = V_{i2}\Big(1 + \frac{R_f}{R_g}\Big) - V_{ref}\frac{R_f}{R_g}. \tag{5.6}$$

This shows that the factor $-V_{ref}(R_f/R_g)$ is added as a bias term to each output voltage. Since $V_{ref}$ was said to be negative, the common mode voltage for each output will increase with this bias term. Although, the bias term will not be present on the differential output voltage which is given by:

$$V_{od} = V_{o2} - V_{o1} = (V_{i2} - V_{i1})\Big(1 + \frac{R_f}{R_g}\Big) - V_{ref}\frac{R_f}{R_g} + V_{ref}\frac{R_f}{R_g} \Rightarrow \tag{5.7}$$

$$\Rightarrow V_{od} = V_{id}\Big(1 + \frac{R_f}{R_g}\Big). \tag{5.8}$$

For this to work, the two gain resistors $R_g$ must be either perfectly matched or the reference voltage must be approximated as infinite impedance. This is to ensure that the common mode current between the two amplifiers stays as close to zero as possible. This means that the reference needs to be buffered with a high impedance, as will be described below.

The negative voltage reference $V_{ref}$ can be created using either a high precision reference component, available in surface mount packages, or by using a voltage division of the negative supply with ground, using only two resistors. In both cases a buffer stage voltage follower (Figure 5.2) is recommended to isolate the reference circuit from the amplifier circuit. If a voltage divider is used, the reference voltage, $V_{ref}$, becomes:

$$V_{ref} = \frac{R_1}{R_1 + R_2}V_{supply}. \tag{5.9}$$

If $V_{supply}$ is negative, the reference also becomes negative as intended.

To stabilize the reference, some design solutions include a decoupling capacitor. If a voltage divider is put directly on the decoupled reference, as in Figure 5.4(left), the transfer function becomes a lot more complicated as it includes the divider resistors and the capacitors at the reference. It will also include the current flowing out of the divider, into the buffer stage. Assuming the two divider resistors, $R_1$ and $R_2$ are equal and name them $R$

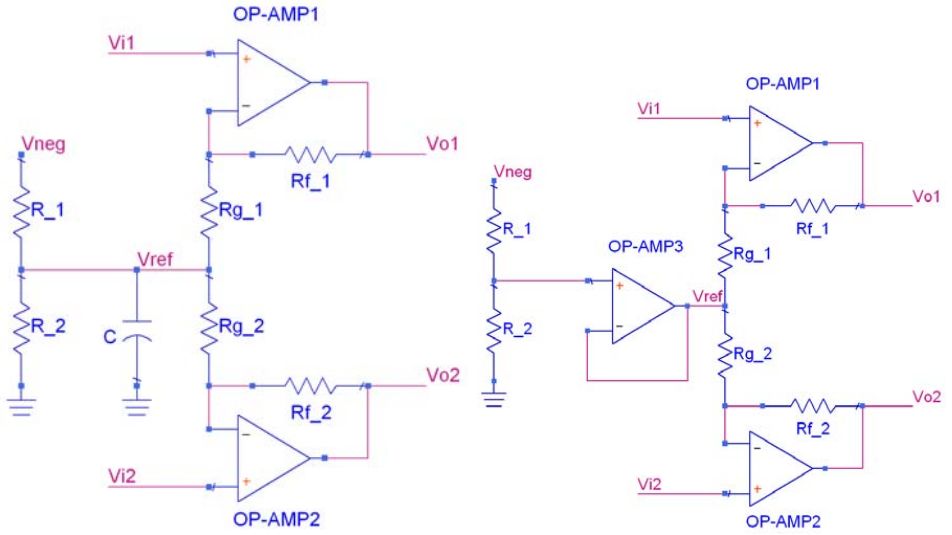


Figure 5.4: Voltage division reference for buffer stages using unbuffered (left) and buffered (right) connection.

and further do a node calculation at the reference node (currents into $V_{ref}$ node equals zero), we get:

$$\frac{-V_{ref}}{R} + \frac{V_{i1} - V_{ref}}{R_g} + \frac{V_{i2} - V_{ref}}{R_g} + \frac{V_{neg} - V_{ref}}{R} - V_{ref} j\omega C = 0, \quad (5.10)$$

$$\Rightarrow V_{ref}\left(\frac{2}{R_g} - \frac{2}{R} + j\omega C\right) = \frac{V_{i1} + V_{i2}}{R_g} + \frac{V_{neg}}{R}, \quad (5.11)$$

$$\Rightarrow V_{ref} = \frac{(V_{i1} + V_{i2})R + V_{neg}R_g}{2R + 2R_g + j\omega CRR_g}, \quad (5.12)$$

where $C$ is the decoupling capacitance, $\omega$ the angular frequency, and $V_{neg}$ the negative supply voltage. The $V_{ref}$, given in Equation 5.12 can be inserted into either of Equations 5.5 and 5.6 to get the voltage at each output, which then is frequency dependent due to the term $j\omega C$. One would now expect from Equations 5.7 and 5.8 that the differential output is independent of the reference voltage, but those equations refer to a constant reference that doesn't change with the input. Equation 5.12 clearly shows that the reference is dependent of the input, and so, Equations 5.7 and 5.8 are not valid. Although, if the reference from the voltage divider is buffered as in Figure 5.4(right), we can approximate the reference to be constant and the term $V_{ref}$ is then simply given by Equation 5.9, a much more simple and reliable design.

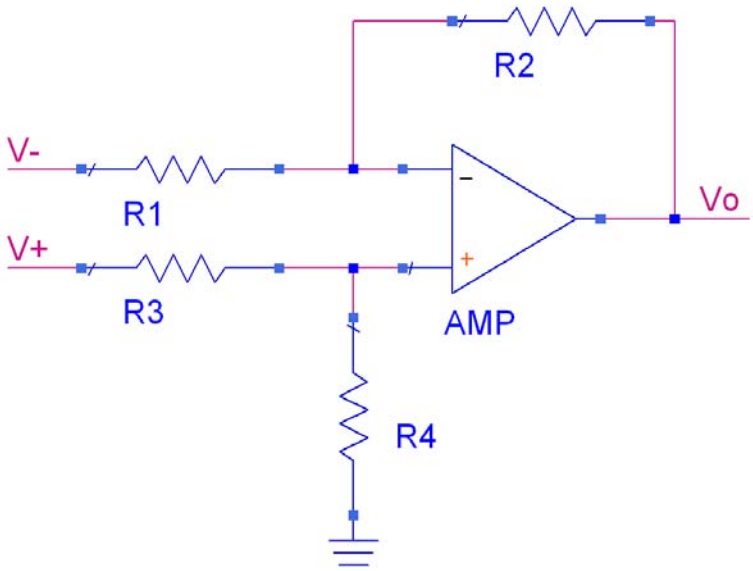


Figure 5.5: Difference amplifier design used as last stage in an instrumentation amplifier.

If the application requires a single ended output, the two buffer input amplifiers are followed by a third operational amplifier. The set up works as a difference amplifier, Figure 5.5. The difference amplifier is very similar to both an inverting and a non-inverting configuration and the transfer function is not straight forward to calculate. We can get the output voltage by using superposition of the results when either input is grounded [14]. When grounding $V_+$ the inverting configuration has output, $V_{o1}$:

$$V_{o1} = -\frac{R_2}{R_1}V_-. \tag{5.13}$$

Grounding $V_-$ gives the non-inverting configuration output $V_{o2}$:

$$V_{o2} = V_+\frac{R_4}{R_3+R_4}\Big(1+\frac{R_2}{R_1}\Big). \tag{5.14}$$

The superposition principle gives that the output voltage $V_o$ is the sum of $V_{o1}$ and $V_{o2}$:

$$V_o = V_{o1} + V_{o2} = \frac{R_4}{R_3+R_4}\Big(1+\frac{R_2}{R_1}\Big)V_+ - \frac{R_2}{R_1}V_-. \tag{5.15}$$

The difference amplifier now amplifies the two input voltages different. This is not a good option as it will result in high common mode amplification and by this poor CMRR. To solve this we set the condition:

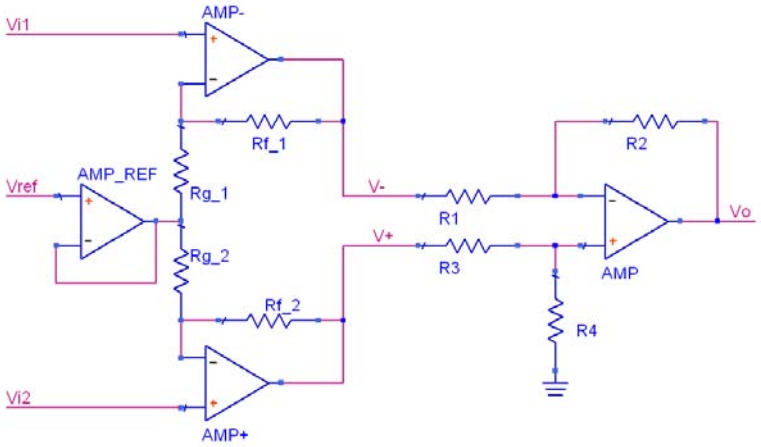


Figure 5.6: A complete instrumentation amplifier with high impedance differential input single ended output.

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}, \tag{5.16}$$

usually by setting $R_1 = R_3$ and $R_2 = R_4$, we get $V_o$ to be:

$$V_o = \frac{R_2}{R_1}(V_+ - V_-) = \frac{R_2}{R_1}V_{id}. \tag{5.17}$$

Now, there is no common mode amplification and the difference amplifier fulfills its purpose. The combination of the difference amplifier and the buffer stage inputs is known as the classic instrumentation amplifier, used in many applications where differential amplification is required. The complete circuit for such an amplifier is shown in Figure 5.6. The total gain of the instrumentation amplifier is found by multiplying Equations 5.8 and 5.17:

$$V_o = \frac{R_2}{R_1}\Big(1 + \frac{R_f}{R_g}\Big)V_{id} \tag{5.18}$$

assuming the condition in Equation 5.16 is satisfied.

In total, three main operational amplifiers has been studied in this thesis. Their performance data are found in Table 5.1 and results from simulations using them in designs are given in Chapter 6.

Table 5.1: Important specifications of op-amps used in buffer stage with ±5 V supply. From data sheets [19] [20] [21].

| Specification | OPA657 | MAX4305 | AD8000 |
|---|---|---|---|
| -3 dB full power bandwidth | 180 MHz | 320 MHz | 650 MHz |
| Input resistance | $10^6$ MΩ | 1.5 MΩ | 2 MΩ |
| Output resistance | 0.02 Ω | 1 Ω | N/A |
| Input capacitance | 4.5 pF | N/A | 3.6 pF |
| Slew rate | 700 V/$\mu$s | 1,400 V/$\mu$s | 4,100 V/$\mu$s |
| Input bias current | ±1.8 nA | ±32 $\mu$A | ±5 $\mu$A |
| Input voltage noise | 4.8 nV/$\sqrt{Hz}$ | 2.1 nV/$\sqrt{Hz}$ | 1.6 nV/$\sqrt{Hz}$ |
| Voltage drift | 12 $\mu$V/°C | 2.5 $\mu$V/°C | 11 $\mu$V/°C |

Table 5.2: Important specifications of LT1993-10 and AD8351 driven with +5 V supply. From data sheets [16] [17].

| Specification | LT1993-10 | AD8351 |
|---|---|---|
| Gain | 20 dB | Configurable |
| - 3 dB bandwidth | 700 MHz | 2.2 GHz |
| Diff. input resistance | 100 Ω | 5,000 Ω |
| Diff. input capacitance | 1 pF | 0.8 pF |
| Diff. output resistance | 0.3 Ω | 150 Ω |
| Diff. output capacitance | 0.8 pF | 0.8 pF |
| Slew rate | 1,000 V/$\mu$s | 10,000 V/$\mu$s |
| Input bias current | ±5 $\mu$A | ±15 $\mu$A |
| $2^{nd}$ HD, 10 MHz | -74/-91 dBc | -70/-90 dBc |
| Noise spectral density, 10 MHz | 1.7 nV/$\sqrt{Hz}$ | 2.65 nV/$\sqrt{Hz}$ |

## 5.3 Differential Amplifier, ADC-driver

Although the differential output of the buffer stage amplifiers could be used to drive a differential AD-converter, it is not the most ideal solution. When interfacing high speed converters an ADC-driving circuit is often required, in the form of a differential amplifier. The ADC-driver has an input pin with a reference voltage, and automatically tries to bias its outputs to this voltage. The reference pin is connected to the ADC common mode output as shown in Figure 5.7, and so there is compatibility between the circuits at all time. The differential amplifiers can also be used as the output stage of an instrumentation amplifier when a differential output is required for some other reason than AD-conversion.

A differential amplifier could be used as a stand alone amplifier stage for the SDTM sensor, but the low input impedance would require matching to the Wheatstone bridge output impedance/resistance including the amplifiers internal impedance. When using buffer amplifiers matching is more straight forward as the input impedance of the device itself is so high that it can be ignored for 50 Ω cases. The buffer stages also give an additional amplification of the weak signal from the sensor.

Two differential amplifiers have been considered here - AD8351 from Analog Devices, and LT1993-10 from Linear Technology. The LT1993-10 has been the preferred choice, since it is highly integrated and has built in tunable low pass filters [16]. The high level of integration makes the LT1993-10 require a minimum of support circuitry, but also means that it has a fixed gain of 20 dB. The AD8351 has its gain set by one or two external resistors, depending on application, and is thus configurable in that sense. A comparison of important specifications for LT1993-10 and AD8351 is found in Table 5.2. This section will only describe the LT1993-10 - as it has been dominating the designs made for the SDTM project. The AD8351 works in a very similar way however.

Figure 5.8 shows the block diagram of the LT1993-10. From the block diagram one sees that the input impedance is quite low (about 100 Ω differential). This is the reason for using the buffer stage described in the previous chapter. Besides the two input amplifiers, A and B, there is a third amplifer, C, that acts as a buffer to the common mode, $V_{OCM}$, input pin. This configuration will bias the output to match the AD-converters inputs. The bias is taken from the AD-converter common mode bias output, $V_{CM}$, as shown in Figure 5.7.

Also seen in the block diagram in Figure 5.8 is the integrated low pass filter at the output of the device. We can actually chose to use the filtered output or the unfiltered output. The filtered outputs will give stable operation with less peaking. The unfiltered outputs are used when the full power bandwidth of the amplifier is to be used. For sensitive instrumentation applications, such as the SDTM, is would be preferred to use the filtered

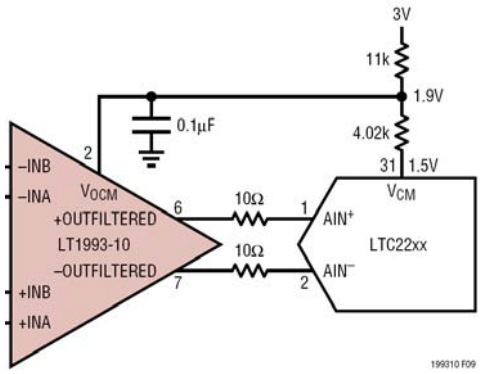


Figure 5.7: How to connect the common mode voltage control between the LT1993-10 and an AD-converter with common mode output [16].

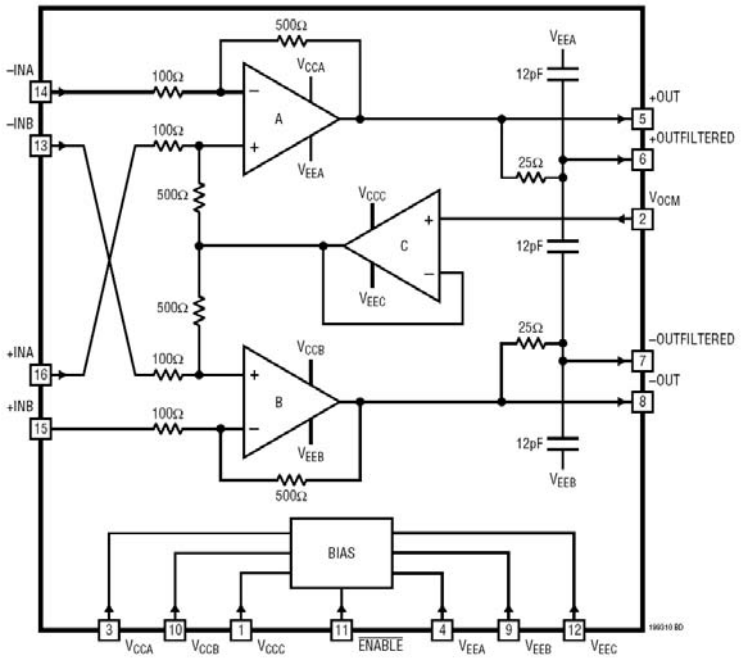


Figure 5.8: Block diagram showing the internal structure of the LT1993-10 differential amplifier/ADC-driver [16].

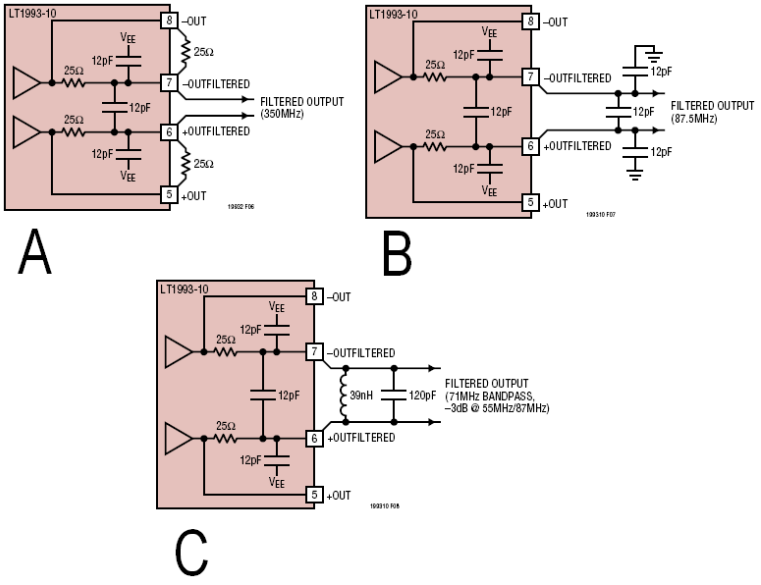


Figure 5.9: Available filter configurations when using the LT1993-10 differential amplifier [16].

outputs, so that the gain remains stable over the whole bandwidth. The filtered outputs use a built in RC low pass filter with one 25 Ω resistor and one 12 pF capacitor at each output. They are also sharing an additional 12 pF capacitor between them to strengthen the balance of the filter. Because of the differential output, the shared capacitor is actually seen as 24 pF, due to the Miller effect[2]. The result is that each output will see a filter consisting of one 25 Ω resistor and a 36 pF capacitor. The -3 dB break point frequency, $f_{3dB}$, of an RC low pass filter is given by:

$$f_{3dB} = \frac{1}{2\pi RC}. \tag{5.19}$$

So by only using the filtered outputs of the LT1993-10 we get $f_{3dB}$ to be about 175 MHz. The internal filters can be configured by external electronics, as shown in Figure 5.9. There are three ways to configure the filters:

**A:** If we want a higher $f_{3dB}$ we connect the unfiltered outputs, $OUT$, to the filtered outputs using a resistor. This resistor will act in parallel to the internal resistor and thus make the total resistance of the filter lower. According to Equation 5.19 this will increase the -3 dB break frequency. Using a 25 Ω resistor for example will double the frequency.

[2]The Miller effect multiplies a capacitor value linearly with the difference in signal amplitude at the capacitor connections. A capacitor between two differential signals are therefore twice the value as it would have had if connected to ground

Table 5.3: Relevant specifications of LTC2255 and LTC2247 ADC:s. From data sheets [22] [23].

| Specification | LTC2255 | LTC2247 |
|---|---|---|
| Sampling rate | 125 MSPS | 40 MSPS |
| Resolution | 14 bit | 14 bit |
| SFDR @ 5 MHz | 88 dB | 90 dB |
| SNR @ 5 MHz | 72.4 dB | 74.4 dB |
| Offset Error | ±2 mV | ±2 mV |
| Full power Bandwidth | 640 MHz | 575 MHz |

**B:** Another tuning option is to connect capacitors to the filtered outputs, either to ground or between them. This will result in paralleling of capacitors which increases the total capacitance seen at the output, thus decreasing $f_{3dB}$ in Equation 5.19.

**C:** If we in addition to one of the above use a high pass filter between the outputs, an inductor for example, we can just as easily create a band pass filter to match a certain application.

Results from various designs, using both the LT1993-10 and AD8351 differential amplifiers, are found in Chapter 6.

## 5.4 Data Acquisition, AD-converter

The ADC LTC2255 selected for the SDTM interface is available from Linear Technology. The ADC can be driven directly with the LT1993-10 ADC-driver described in the previous section, making it a good choice for simplicity. The performance sets a typical balance between speed and resolution. Besides the LTC2255, a similar, but slower ADC has also been studied. This ADC, LTC2247, has been available as an evaluation board, manufactured by Linear Technology. The evaluation board houses all the hardware and software for taking and analyzing a single analog signal, as it isn't differential. Performance for both converters are found in Table 5.3. Performance measurements for the LTC2247 using various clock sources are found in Chapter 6.

First let's take a look at the performance required of the ADC inherited from the requirements given in Chapter 2. The bandwidth was there set to 500 MHz. The highest resolvable frequency, $f_{max}$, in relation to the sampling frequency, $f_{sample}$ is given by the Nyqvist theorem:

$$f_{max} = \frac{f_{sample}}{2}. \tag{5.20}$$

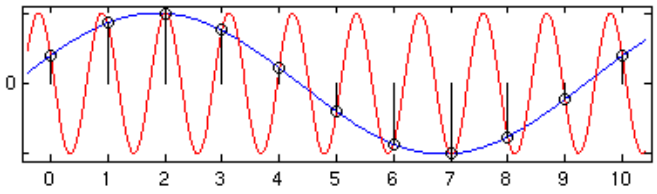


Figure 5.10: Undersampling of frequency above the Nyquist frequency gives aliased result. Image from Wikipedia.

This is not a realistic target, as the fastest converters available off the shelf today can be clocked to work around 150 million samples per second (MSPS), making the highest resolvable frequency to about 75 MHz. At least this is the case for continous measurements over the whole frequency range. Higher frequencies can be resolved if they are limited in a narrow band pass. This is because aliasing will mirror the measured frequency around the Nyquist rate (half the sampling rate). This comes from the fact that two frequencies can give the same sample points if one of them is higher than the Nyqvist frequency, as seen in Figure 5.10. This is frequently used in telecommunication applications where the signal power of a known frequency component, in the MHz/GHz range, is to be converted with standard low cost ADC:s.

When working with regular conversion applications it is noticeable that aliasing causes problems even when measuring in a bandwidth less than Nyquist. These problems occur when high frequencies are not filtered sufficiently, and so appear in the lower bands due to aliasing. This is usually handled with anti-aliasing filters. These filters should have very sharp low pass cutoff points to maximize the usable bandwidth. The problem can also be approached by oversampling, where the filtered bandwidth is far below the Nyquist. Oversampling also increases the signal to noise ratio (SNR), since there are more samples that can be averaged.

The next important requirement in Chapter 2 was the field range and resolution. These are closely related since their ratio determines the minimum resolution of the ADC. For the SDTM the following was given:

- Field range: 65 $\mu$T
- Resolution: 3 pT

The ratio of the field range and the resolution gives the number of required steps to resolve. In this case this equals about 22 million steps, in the following denoted as $Q$. The number of bits, $N$, required for this is given by,

$$2^N = Q \Rightarrow \tag{5.21}$$

$$N = \log_2 Q = \frac{logQ}{log2}. \tag{5.22}$$

For the SDTM requirements, this would require a 25 bit converter. Although such a converter can be found, it is likely to be slow or very expensive. Off the shelf ADC:s in the range of 100 MSPS or higher have resolutions up to 14 or 16 bits. Using averaging, the resolution can be increased with oversampling, but of course with the cost of much lower sample rate. It is inevitable that higher sampling rate decreases the resolution and vice versa, because of noise floor limitations. One must therefore usually choose between high sensitivity and high speed in an analog to digital conversion system.

High performance ADC:s use a sample and hold (S/H) concept when measuring the signal. This means that the input will track the voltage for a short sample period and then hold this value until it has been transfered to the converter circuitry. The S/H technique allows for high sensitivity since it remains at the same value throughout the transfer period, thus limiting quantization errors that occur when tracking continue during the transferring.

# Chapter 6

# Achievements and Results

The results in this thesis are scattered over many regions, connected by the intention of developing highly sensitive electronic devices for the SDTM project. This chapter will present achievements done during the work, such as design processes, concepts and solutions. The final part of the chapter will present the resulting designs made for the SDTM system, along with some important performance characteristics.

## 6.1 SDTM prototype circuit board concepts

When evaluating the electronic components used in the SDTM design there are two important aspects to remember. The prototyping needs to be easily configurable and require the least amount of repair and redesign time as possible. At the same time, the highly sensitive components have to be used with circuit boards having the proper design approaches for grounding, decoupling, EMC and shielding. These two aspects, of simplicity and compatibility, unfortunately do not always work well together. This has been a hard lesson learnt during the thesis work.

Two concepts of prototyping have been considered and carried out. The first one was to build all parts of the electronic on small modules. This is called the *Modular Design Concept*. Each such module has a certain set up of electronics that carries out a specific function in the whole system, such as buffering, amplifying, power supply, interfacing and filtering. This concept works good in theory as it takes away the situation where a small layout fault or electronic malfunction in a design necessitates a complete rework of the circuit boards. The drawback is that many of the important considerations described in Chapter 4 are not taken into account. For instance, the modules connect to each other through a standard breadboard, and thus removing the entire concept of using an unbroken ground plane for the whole analog signal processing system.

A typical problematic setup, using modules is illustrated in Figure 6.1. It

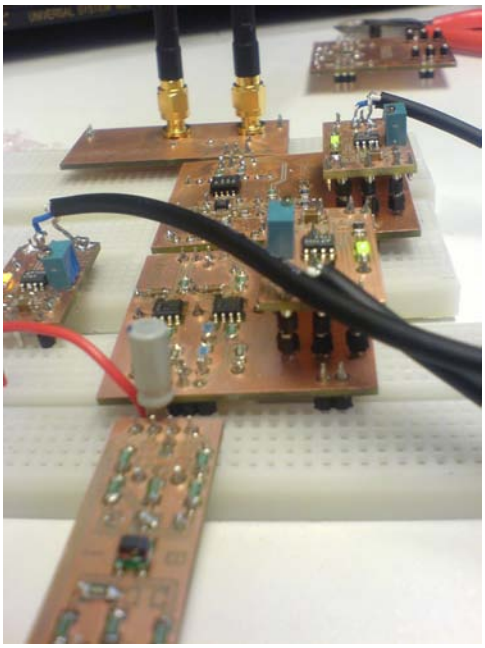

Figure 6.1: Typical measurement setup for the modular system concept, clearly showing the problems encountered with grounding and long trace distances.

is not difficult to understand the upcoming problems with ground errors and circulating currents that appear when this is run at high frequencies. One would think that the problem can be solved by limiting the input frequency range, but it is then important to remember that the high bandwidth components, such as the LT1993-10 described in Chapter 5, will still amplify high frequency noise content. Noise amplification combined with ground current problems can then lead to instability and oscillations in the circuits. EMC problems are also common in oversized designs, for example, one setup gave the spectrum seen in Figure 6.2 showing peaks corresponding to Swedish national radio frequencies, as a result of ground pick-up. The setup was here similar to the one in Figure 6.1. The main approach towards the ultimate system design for the SDTM has followed the concept of modular designing. Even though these modules have shown poor performance, most likely because of the aspects mentioned, they have provided important results for a final design.

The other concept was to build prototype integrated circuit boards, either on two-layer circuit boards available instantaneously within the Ångström laboratory using IRF's circuit board plotter, or by ordering multi-layered printed circuit boards from a manufacturer. The main advantage of using an integrated design is that the high speed laws for circuit board layout can be properly addressed. The concept also makes the prototypes smaller, and

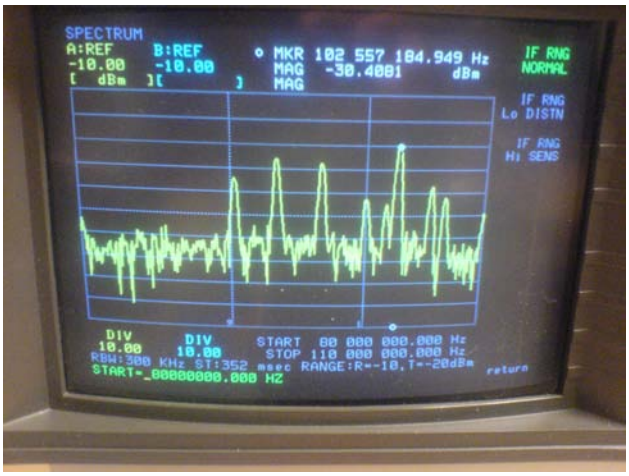


Figure 6.2: Radio station pick-up when using modular circuit boards. Detected with spectrum analyzer.

easier to handle, shield and integrate with other designs. On the other hand the concept requires thorough and well thought through layout and design work. A single mistake can make the whole circuit useless, which would waste a lot of money if the circuit boards are ordered from a manufacturer. Integrated designs have not been tried out much here, but in a sense the individual modules in the modular design concepts can be considered being integrated designs. As many of the modules have been thoroughly tested and evaluated, the concept of integration is known to pay off in the end.

## 6.2 Manufacturing processes and design considerations

The manufacturing processes have shown themselves reliable enough for making good two layer prototype circuit boards. They are well suited for rapid prototyping of experimental circuit boards, but are not recommended as the final solution when starting to consider integration and performance optimization. Some of the results and achievments have already been presented in Chapter 3, and are further described in Appendices B and C

The processes and skills achieved during this thesis are the following:

- Establishing electronic drawing and simulation knowledge through extensive work with the software *Advanced Design System*, from HP/Agilent. A comprehensive tutorial for the software is found in Appendix B.
- Establishing routines and design restrictions for manufacturing prototype circuit boards, using the *LPKF S62 Circuit Board Plotter*. A

tutorial for the mill and its control software is found in the first part of Appendix C

- Developing processes for solder paste screen printing using Kapton™ film as stencil material and the LPKF mill for manufacturing. More about this is found the last part of Appendix C

- Developing reflow soldering temperature profiling and equipment selection for proper soldering. More about this is also found in Appendix C.

One important improvement when making circuit boards is the use of plated via holes in circuit boards. The pin through and hand soldered vias, used throughout this thesis are thought to be a reason for some electromagnetic interference pick-up. There are many different options for plating, one being by ordering printed circuit boards directly from manufacturers, the other to use small rivets, available off the shelf. This is a good solution for two layer prototype circuit boards. The rivets are placed on circuit boards using a special tool, and then soldered by hand, giving the circuit board a much lower profile and so making it less susceptible to electromagnetic pick-up, by minimizing the small "antennas" appearing everywhere on the board otherwise.

Besides vias, the total size of circuit boards have to be kept at a minimum. Electric distances over an entire system should not exceed a fourth of the maximum wavelength passing through a system to avoid mismatch reflections and resulting losses in stability and efficiency. Most of the circuit boards designed and built during this thesis have not been integrated enough, and many problems have occurred, that could have been eliminated. High integration and short trace distances, combined with better via plating, will most probably require manufactured printed circuit boards. Only simple, low speed, experimental or digital circuit boards should be made by milling out prototypes. In addition, the ordered printed circuit boards should also be configured in several layers. The use of multi-layered printed circuit boards will introduce the ability to use power and ground planes more extensively. Besides removing traces from signal planes, this will allow for designs with low impedance power supply and completely unbroken ground planes, thus improving performance and stability. Multi-layering will also allow for a higher degree of integration and more flexible placement of component and signal traces, as there will be more space available on these planes.

Improvements can also be achieved by using smaller discrete components, such as resistors and capacitors. These are today available in 1206 packages only, making them larger than most other components in the designs, including the relatively large AD-converters. The 1206 can be replaced by 0603 or even 0402, greatly improving the ability to reduce the size of designs.

It has clearly been proven, throughout the thesis, that building high speed electronics requires integrated an careful layout work. The modular

design experimented with throughout the thesis is appropriate for testing and evaluation of components and discrete parts of the system, but can simply be considered a bad choice for the ultimate SDTM electronic system. Even so, the modular circuit boards manufactured have provided excellent results when tested individually. Thanks to these numerous designs, several parts of the whole electronic system has been tested and proved to fit most requirements.

## 6.3 ÅSTC laboratory equipment

As mentioned, one part of the thesis has been to evaluate the capabilities of the ÅSTC laboratory and the equipment available. By using the equipment regularly for the several months, it is clear that some improvements will be necessary. A few examples of problems encountered are: power supplies with output voltage errors, slow and unstable oscilloscopes and a sine wave signal generator unable to output more than 2 MHz.

An equipment upgrade would be relatively expensive, so the cost must be weighted against the intended future projects under consideration. The investment should in the end depend on the intentions within the research group. High performance electronic, especially when including high frequencies, require proper equipment for testing and verification. If this is not available, the development slows down considerably, as equipment for these tasks has to be found somewhere else.

## 6.4 Electronic designs and performance

This section, with its subsections, contains circuit boards and design solutions, that have worked and proved reliable, and are of importance for future integration of the SDTM signal processing and data acquisition system. Circuit boards have been milled with the ProtoMat S62 mill from LPKF AG. Drawings, CAD layouts and simulations have been made using Agilent/HP Advanced Design System (ADS). Signal and transmission measurements have been made using the Tektronix TDS210 Oscilloscope and the HP 4195A Network/Spectrum Analyzer. Both have had the possibility of transferring data to a connected PC. Performance measurements for Analog to Digital Converters have been done using a data acquisition board with bundled control software from Linear Technology.

### 6.4.1 Bias module

The bias module provides low noise and stable voltage when connected to a circuit. The DC/DC converter used is the LT1763 from Linear Technology. The regulation is done using a voltage divider, connected to the circuit. The

converter then tries to keep the mid-divider voltage at 1.22 V, thus creating a current over the resistor tied to ground. Depending on this resistor value, the output is set accordingly. On the circuit board, the voltage divider is represented by an adjustable resistance (potentiometer). The output voltage can be tuned between 1.22 V and $V_{in}$ by turning the potentiometer. The potentiometer turns up to 20 revolutions and the voltage can therefore be set very precisely. A large decoupling capacitor at the output ensures stability and a surface mounted LED[1] indicates operation. The noise figures for the bias module (Figure 6.3, operating at 5V input and 2.5V output, are shown in Figure 6.4. The reduction in noise is found by taking the ratio of the standard deviation or the variance of the regulated and unregulated supply. The input power supply had a standard deviation of 1.205 mV and the regulated LT1763 output 0.835 mV during the measurements, giving a noise figure ratio of 0.69, a 45% improvement. If instead the variance is used, the improvement is the square of this, giving a ratio of 0.48 (halving the noise).

This bias module has proven very reliable and has been used to power most other modules. The low output noise and the possibility to place it in close proximity to circuits, thus removing cabling EMC, has been very valuable through the work.

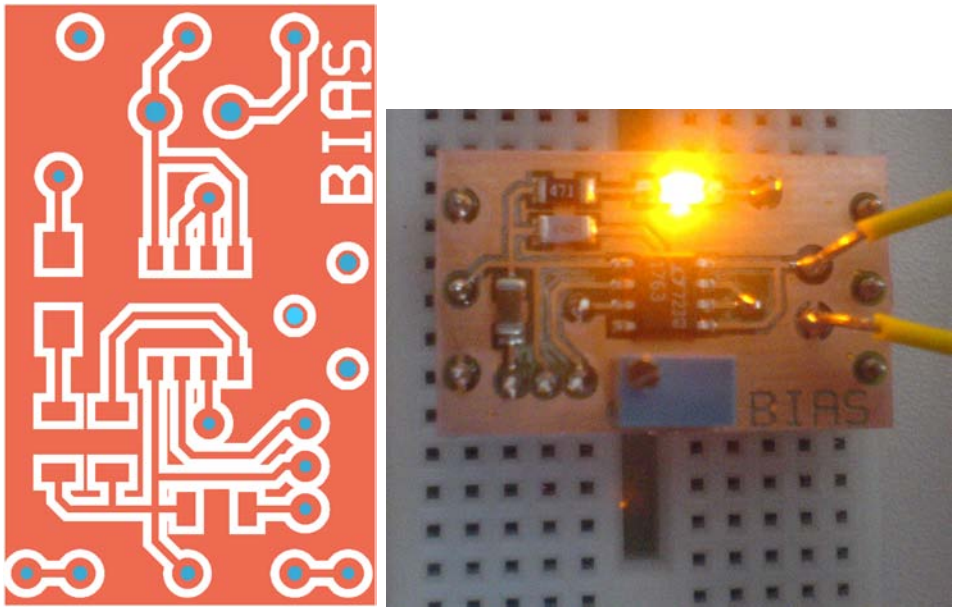


Figure 6.3: Bias voltage module circuit board. Utilizing the LT1763 DC/DC converter.

[1] Light Emitting Diode

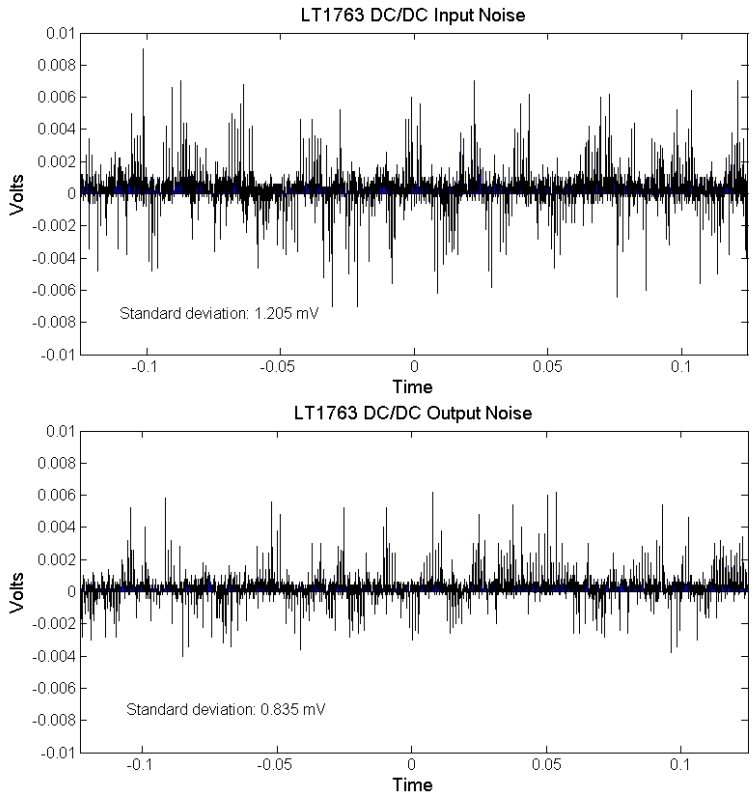


Figure 6.4: Comparison of noise figures when using the LT1763 DC/DC converter. Upper image shows unregulated noise, and the lower the regulated output from the device.

### 6.4.2 Balun transformer

Balun transformers are used in high frequency applications to transform single ended signals to differential or the other way around. The basic configuration is shown in Figure 6.5. The figure shows that three connections are used at one end of the transformer to create or accept a balanced differential signal. The center tap should be connected to the signal common mode reference for proper operation. For a signal balanced around zero volts, the tap is connected to ground. The other end has two connections that allow, or provides, single ended signaling. Besides being used as a single ended to differential converter, the balun is also practical to use when trying to match impedances between different systems. The balun isolates, impedance wise, two systems from each other, thus providing simpler approaches for matching.

Several module circuit boards using high bandwidth baluns have been built for this thesis. A detailed picture from one of these circuit boards, using the balun CX2156, is found in Figure 6.6

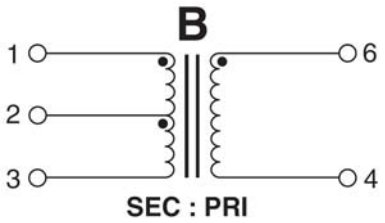


Figure 6.5: Principal schematic of balun transformer.

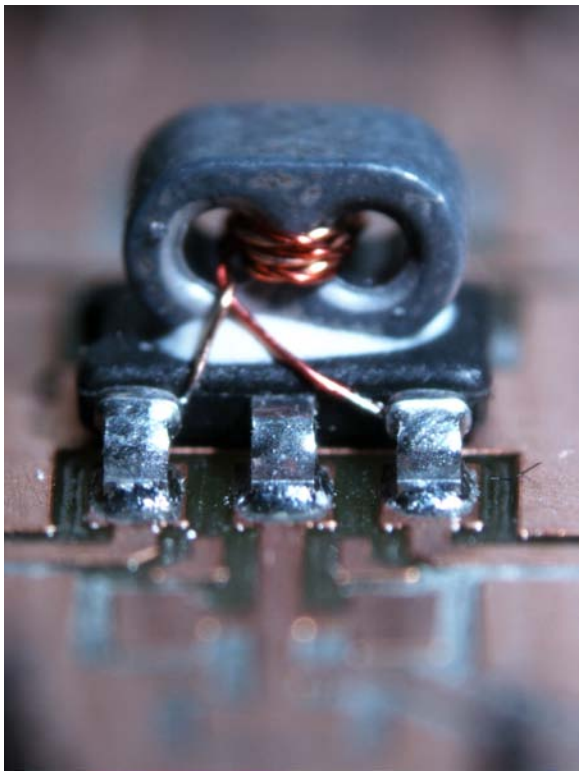

Figure 6.6: CX2156 balun on circuit board.

### 6.4.3 Magnetometer

As a replacement for the SDTM magnetometer, being under development at ÅSTC, a commercial sensor has been used. Figure 6.7 shows an integrated circuit board for the AAL002 sensor from NVE Corporation. The circuit board incorporates the LT1763 DC/DC converter to stabilize the Wheatstone bridge bias voltage, and to allow adjustments being made on the bias directly. Because a suitable magnetic field generator has not been available, no frequency limitations have been measured for this circuit. Figure 6.8 shows a snapshot capture of the differential output from the sensor when

stimulated manually by a strong magnet. The measurements were done for both 5 V and 1.22 V bias voltage. The unsymmetrical behavior of the signal is from because of the wobbling rotation of the stimulating magnet, but the distinct differential behavior is clearly visible.

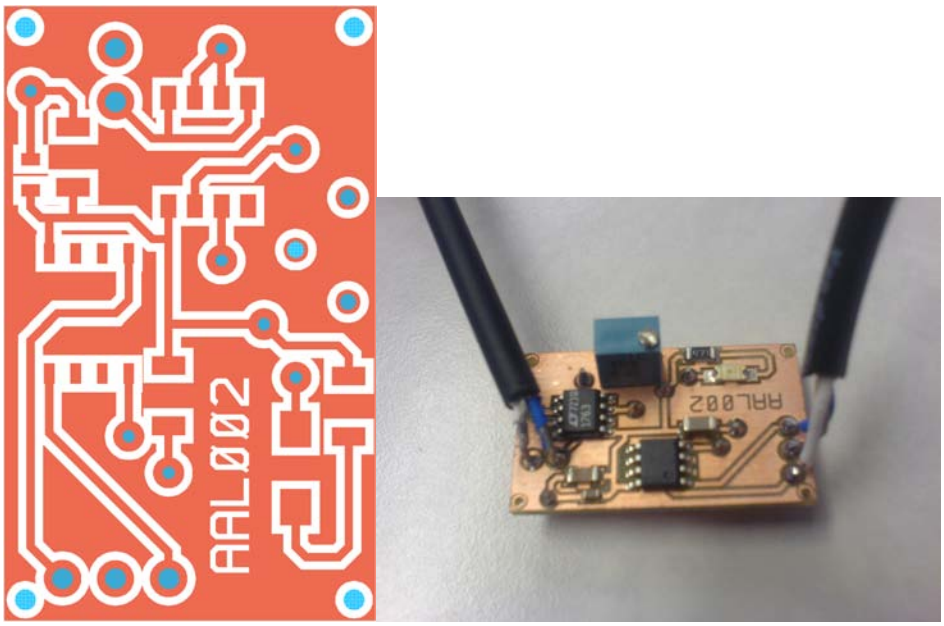


Figure 6.7: Schematic and picture of the integrated AAL002 circuit board.

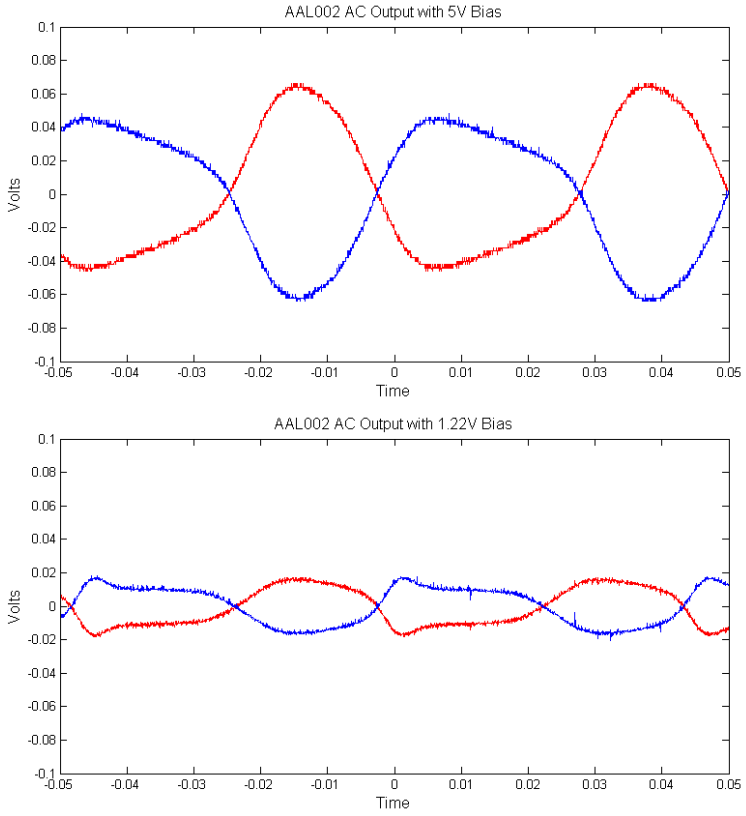


Figure 6.8: Differential output from the ALL002 magnetometer when stimulated by a rotating strong magnet. Upper image when biased by 5 V and lower image when biased by 1.22 V.

### 6.4.4 Buffer stages

The buffer amplifier input stages built and designed during the thesis are intended to be used as low noise pre-amplifiers for the magnetometer. Ideally they are set up as in described in Chapter 5, using two operational amplifier that isolates and amplifies the differential signal coming from the Wheatstone sensor. This differential buffer stage is commonly used as the input stage to an instrumentation amplifier, where the output stage is either a difference operational amplifier or a differential amplifier, depending on application.

Two buffer circuit boards have been built during the thesis, using the MAX4305 and AD8000 operational amplifiers. The AD8000 circuit board is found in Figure 6.9. They do not implement the design of the instrumentation amplifier, described in Chapter 5, instead they are configured independent of each other. This limits the possibility of using them together with the sensor, but greatly improves characterization and measurements of the buffer stages themselves, since balancing requirements are absent. Both

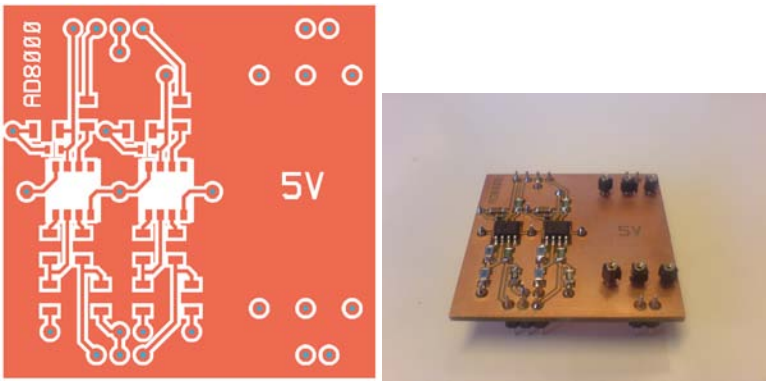


Figure 6.9: AD8000 buffer circuit board.

circuit boards were run through the network analyzer at IRF, but failed to give the expected performance. Although, the worked during basic testing with an oscilloscope, but without the expected gain. The reason for these bad results are not fully understood.

Even if the built buffers have shown problematic behavior, the simulation results for various operational amplifiers are promising. When using the circuit in Figure 6.10 for the MAX4305 and the high impedance FET-input OPA657, the results show bandwidths exceeding several hundred MHz for the MAX4305 and at least 150 MHz for the OPA657, as seen in Figures 6.11 and 6.12. Even if the later shows much lower bandwidth, its high impedance inputs are ideal for use in a buffer configuration. The use of a reference voltage in these simulations, are to test the ability of the stage to operate together with a single-supply differential amplifier.

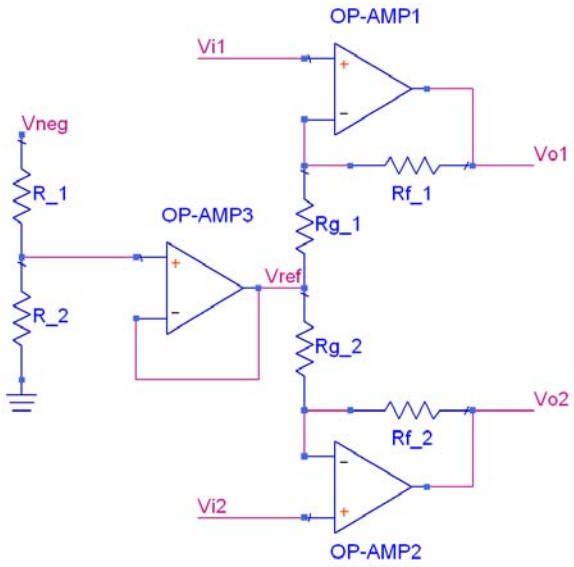


Figure 6.10: Simulation schematic of input buffer stages for use with the OPA657 and MAX4305 SPICE models.

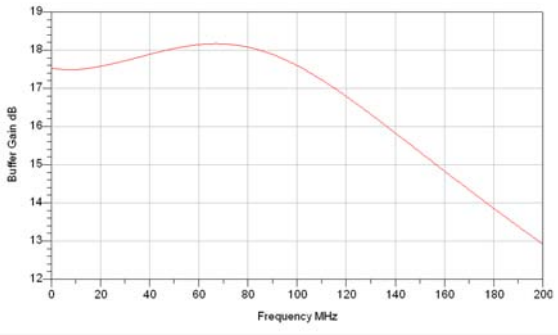


Figure 6.11: Simulation results of OPA657 input buffer.

### 6.4.5 Differential amplifiers

The differential amplifiers used are mainly intended to be used as front-ends to AD-converters requiring differential input signals. The differential amplifiers are similar to other amplifiers, but give a differential output balanced around a certain common mode voltage. The circuits usually have integrated common mode biasing and feedback, so the required external circuitry is limited - making them very useful for highly integrated designs. This also means that a differential signal can be inserted directly into the device, requiring no input networks, except the required terminations.

Two circuit boards using differential amplifiers have been built. One using the LT1993-10 circuit from Linear Technology and one using the AD8351

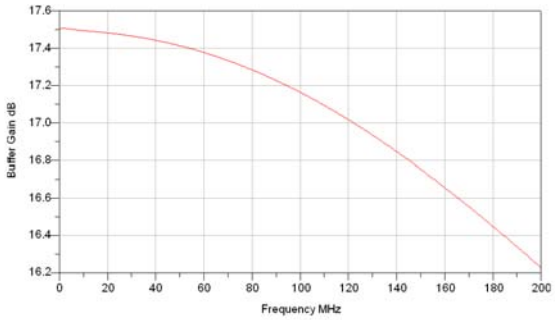


Figure 6.12: Simulation results of MAX4305 input buffer.

from Analog Devices.

The AD8351 is most similar to an operational amplifier, as it requires an external gain resistor, and when driving a single-ended output, also a feedback resistor to ensure stability. The common mode level is still set internally by connecting the VOCM pin of the device to the common mode required. A circuit board using the AD8351 is found in Figure 6.13 and the transfer function, measured on a network analyzer, in Figure 6.14. The measurements show great bandwidth, even with a relatively large circuit board. About 250-300 MHz is easily achieved. No model for the circuit was available from Analog Devices, so much required simulations for various configurations could not be done. Instead trial and error had to be used to find a good configuration.

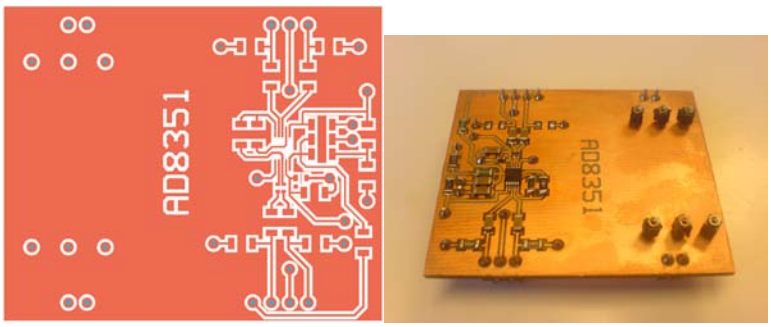


Figure 6.13: AD8351 module circuit board schematic and photo.

The LT1993-10 is the more advanced solution. As described in Chapter 5, it has integrated feedback and a fixed gain of 20 dB, and also utilizes an internal differential low pass filter, that can be configured with the use of external components. The circuit board, using the LT1993-10 is found in Figure 6.15. The LT1993-10 should, according to specifications, be superior to the AD8351 in most applications, but has proved very unreliable and unstable during testing. Many circuit boards using the device have failed

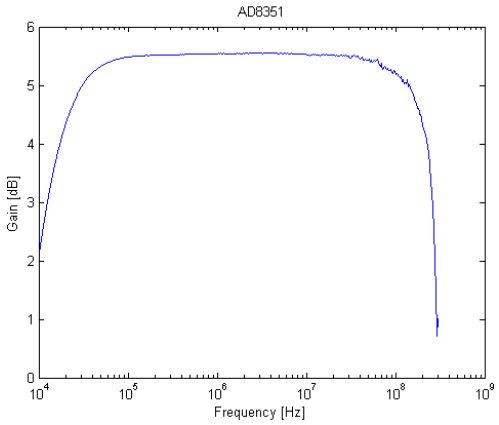


Figure 6.14: Network analyzer result with the AD8351 module circuit board.

to work, oscillated or behaved generally unstable. The network analyzer measurement result in Figure 6.16 clearly shows instabilities and extensive peaking at high frequency. The extensive peaking happens when the device reaches its resonant frequency and starts amplifying signals 180° out of phase. Since the feedback network is integrated, these resonances cannot be altered by changing the feedback transfer function. Even so, the network plot shows the possibility of the device working above 300 MHz if resonances are suppressed somehow. Simulations of the LT1993-10 show great performance, with a bandwidth exceeding 500 MHz, providing a stable transfer function, as seen in Figure 6.17.

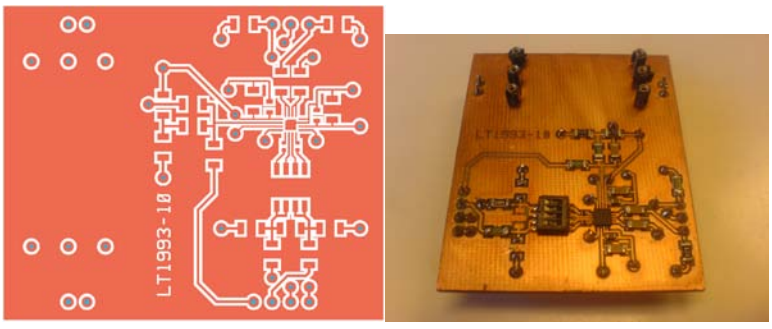


Figure 6.15: LT1993-10 module circuit board schematic and photo.

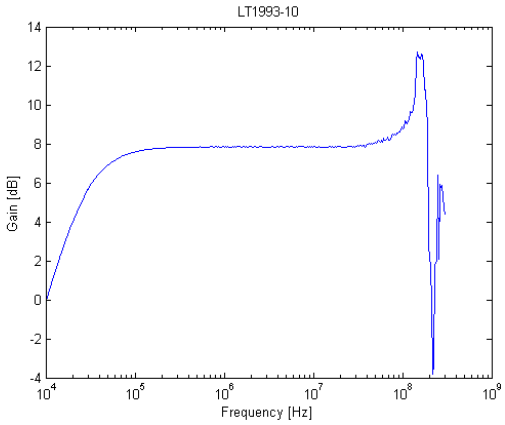


Figure 6.16: Network analyzer result with the LT1993-10 module circuit board.

### 6.4.6 AD-converter and data acquisition

The LTC2255 converter from Linear Technology, mentioned in Chapter 5, has been the primary choice during the project. Especially because of the high sampling rate and resolution. A circuit board designed for the LTC2255 is found in Figure 6.18. Although, due to lack of time, and the importance of other tasks, the circuit board has not been built and the LTC2255 therefore not tested. Instead, a slower converter, LTC2247, was acquired pre-built from the manufacturer, this evaluation board came bundled with a high speed data acquisition board. Both of these circuit boards are shown in Figure 6.19.

The acquisition board is connected to the computer via an USB interface and controlled with a designated software package available from Linear Technology. Running these high speed converters at maximum sampling speed creates a lot of data in a short time, and must therefore be addressed properly. At full speed the bandwidth required is the resolution times the sampling rate - for the LT2247 this equals 14x40E6 = 0.56 Gbps. For the LTC2255, which can be connected to the same data acquisition board, the required rate would be 14x125E6 = 1.75 Gbps. These rates cannot be transferred in real time over the USB interface, so a "burst mode" implementation is used during the conversion phase. During burst mode, data is stored locally on the data acquisition board on high speed memory chips. When the sampling is complete, the data is transferred to the computer at whatever speed is available. The limitation of the entire system is that the data acquisition board can only make data burst measurements using its internal memory. For our 14 bit AD-converters, the maximum number of sequential measurements that can be stored on this memory is 9362. If 40 Msps is used, the measurement period would only be 234 $\mu$s. The short measurement pe-

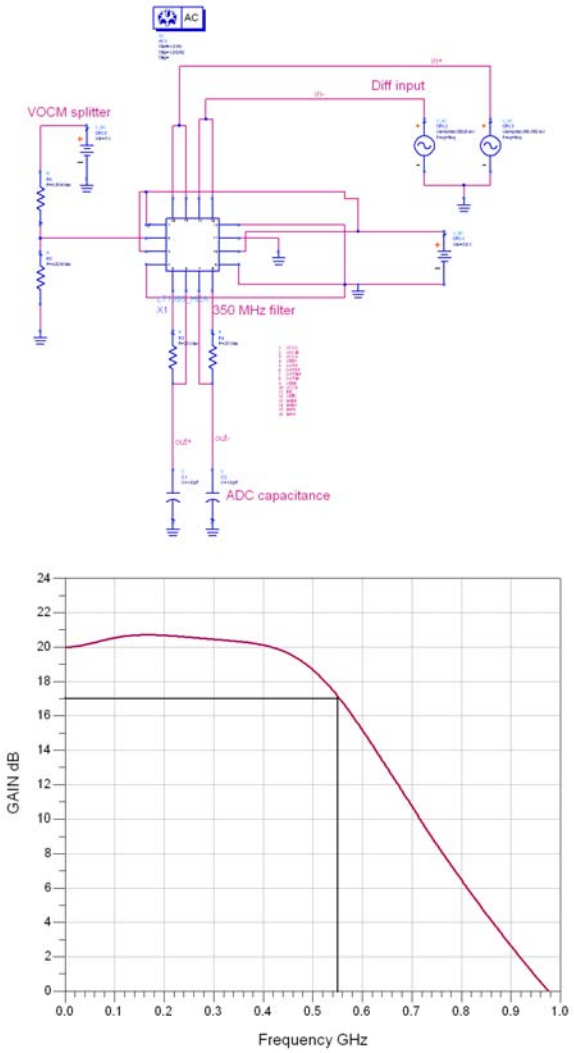


Figure 6.17: LT1993-10 550 MHz simulation circuit and graph.

riod limits the lowest resolvable frequency, and the data acquisition system is therefore bandpass limited.

The converter circuit board has no built in clocking device, so this has to be connected externally. There has been two solutions for the clocking of the device. The home made clocking solution uses a temperature controlled oscillator, VM57T3, with a TTL standardized output and is available from Mercury Electronics. This oscillator is very stable due to its built in temperature compensation and drifts only a few ppm[2] in output frequency. Two versions have been built, one with a 8.192 MHz output and one with a 38.8

[2]part per million

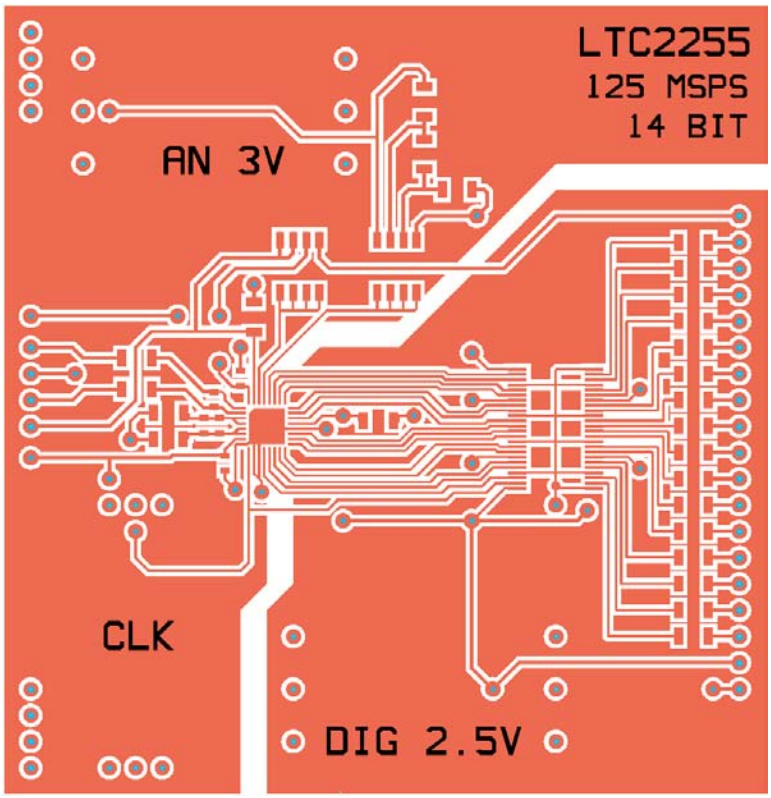


Figure 6.18: Circuit board layout for use with the LTC2255 high speed AD-converter.

MHz. The circuit board is found in Figure 6.20 and has been used successfully to clock the LTC2247. The output waveforms from the two versions of the board is found in Figures 6.21 and 6.22.

The second solution to clock the converter has been by ordering an evaluation circuit board from a manufacturer that could be more precisely controlled. Fortunately, another group within ÅSTC had done precisely this, and were kind enough to let it be used by the SDTM project. The evaluation board CLK5620 from Lattice Semiconductor Corp. also uses bundled software to give a precise low voltage TTL or CMOS output. This board is shown in Figure 6.23 along with its output waveform at 40 MHz in Figure 6.24.

The measured performance of the LTC2247 evaluation board are found in Table 6.1. Measurements were done at 2 MHz (1 V), 2 MHz (200 mV) and 50 kHz (1 V) input, using three clock configurations: The CLK5620 at 40.0 MHz, the VM57T3 at 38.8 MHz and the VM57T3 at 8.192 MHz. The results are similar for almost all measurements, showing only a slight

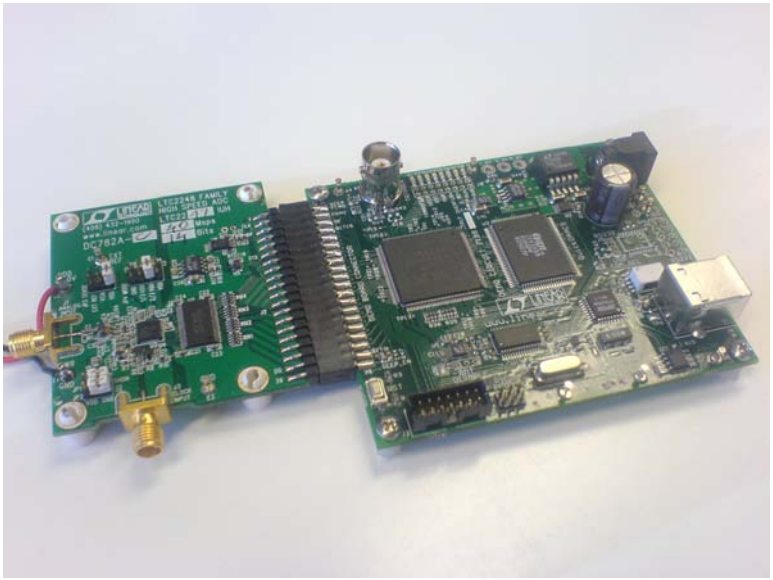

Figure 6.19: Evaluation circuit board of the LTC2247 AD-converter attached to high speed data acquisition board.

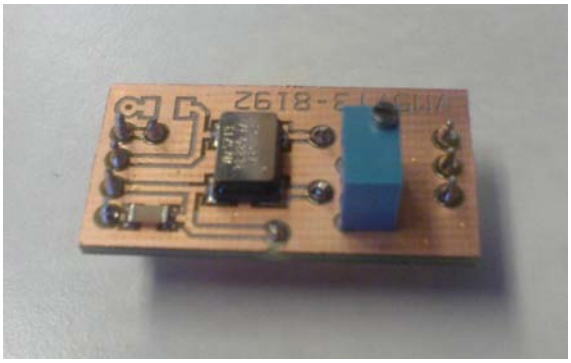

Figure 6.20: TTL clocking circuit using the VM57T3 high precision, temperature compensated, clock from Mercury electronics.

improvement in SNR[3] for the CLK5620. THD[4] and SFDR[5] are almost equal for all clocks, input voltages and frequencies. Because of the balun transformer input stage of the AD-converter circuit board, the 50 kHz input gave a lower amplitude of the signal, but the SNR remained almost unchanged. The only abnormality was that the measurements using the CLK5620 at 50 kHz had enormous harmonic amplitudes and significantly higher noise than the other measurements and so resulted in very poor THD and SNR. If com-

[3]Signal to noise ratio
[4]Total Harmonic Distortion
[5]Spurious Free Dynamic Range

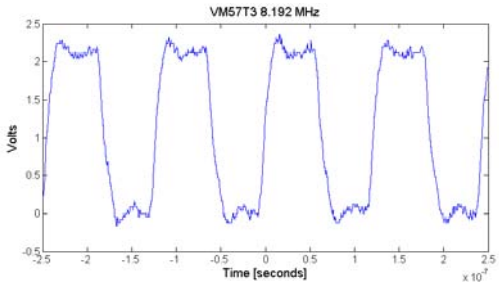


Figure 6.21: Output graphs from the VM57T3, 8.192 MHz version.

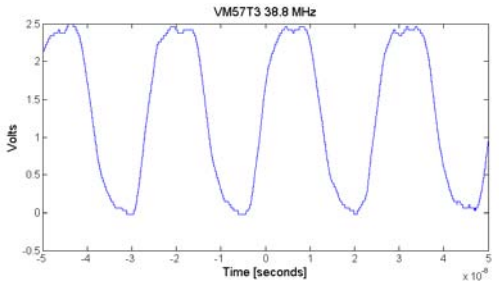


Figure 6.22: Output graphs from the VM57T3, 38.800 MHz version.

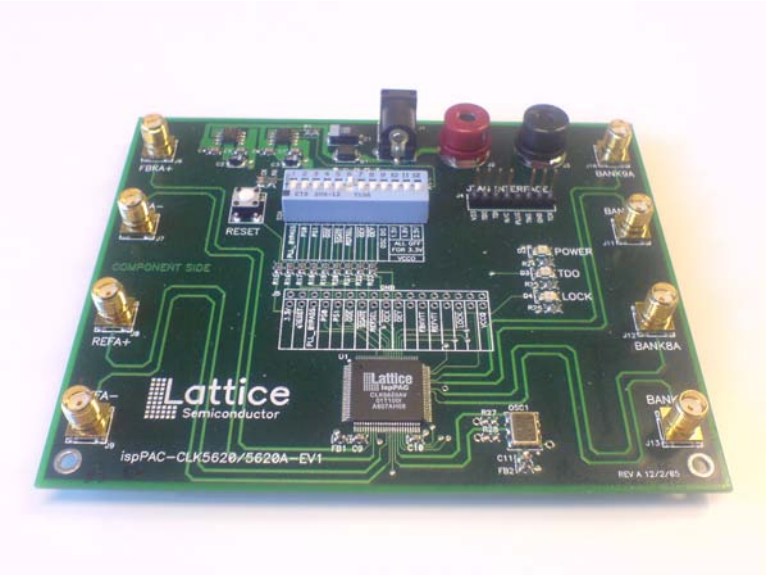


Figure 6.23: 40.0 MHz output waveform from the CLK5620 evaluation circuit board from Lattice semiconductors.

pared to the idealistic figures given in the LTC2247 data sheet, the results may seem terrible, but it is important to remember that such figures are

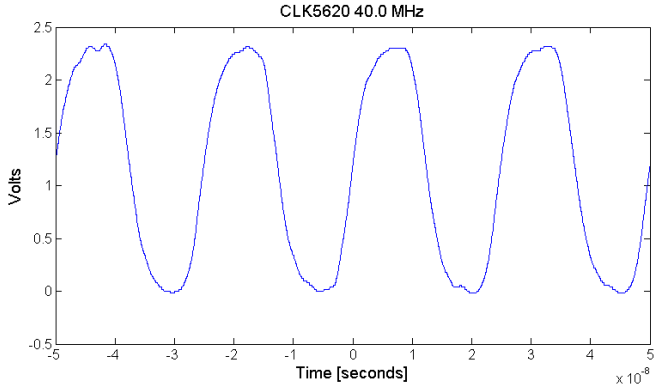


Figure 6.24: 40.0 MHz output waveform from the CLK5620 evaluation circuit board from Lattice semiconductors.

often taken under conditions usually not available in standard laboratories.

Since the input stage of the LTC2247 is differential, but the circuit board uses a balun transformer so that single-ended signals can be used. This makes it problematic to interface to differential amplifiers. The final AD-converter circuit board should contain differential inputs to maximize performance.

Table 6.1: LTC2247 ADC evaluation board performance data.

| | 2 MHz 1 V single tone | | |
|---|---|---|---|
| Clock | VM57T3 | VM57T3 | CLK5620 |
| Frequency | 8.192 MHz | 38.800 MHz | 40.000 MHz |
| F0 [dBFS] | -12.575 | -12.561 | -12.659 |
| F1 [dBc] | -31.41 | -31.41 | -31.83 |
| F2 [dBc] | -34.23 | -33.89 | -33.04 |
| F3 [dBc] | -48.54 | -47.37 | -48.15 |
| SNR [dB] | 40.61 | 40.92 | 41.81 |
| THD [dB] | -29.42 | -29.32 | -29.26 |
| SFDR [dB] | 31.41 | 31.41 | 31.83 |
| | 2 MHz 200 mV single tone | | |
| Clock | VM57T3 | VM57T3 | CLK5620 |
| Frequency | 8.192 MHz | 38.800 MHz | 40.000 MHz |
| F0 [dBFS] | -29.955 | -28.052 | -27.826 |
| F1 [dBc] | -29.01 | -29.08 | -29.61 |
| F2 [dBc] | -37.62 | -35.88 | -32.61 |
| F3 [dBc] | -49.08 | -51.29 | -51.59 |
| SNR [dB] | 23.35 | 27.45 | 27.70 |
| THD [dB] | -28.40 | -28.21 | -27.81 |
| SFDR [dB] | 29.01 | 29.08 | 29.61 |
| | 50 kHz 1 V single tone | | |
| Clock | VM57T3 | VM57T3 | CLK5620 |
| Frequency | 8.192 MHz | 38.800 MHz | 40.000 MHz |
| F0 [dBFS] | -19.782 | -21.028 | -20.402 |
| F1 [dBc] | -39.85 | -39.69 | -14.74 |
| F2 [dBc] | -44.10 | -38.01 | -23.72 |
| F3 [dBc] | -55.58 | -50.96 | -48.95 |
| SNR [dB] | 43.31 | 39.70 | 16.69 |
| THD [dB] | -38.95 | -35.32 | -14.22 |
| SFDR [dB] | 39.85 | 38.01 | 14.74 |

# Chapter 7

# Conclusions

The electronic modules achieved during this thesis have, with a few exceptions, provided excellent results and proved to be operational. Although, the have not worked very well together. But, in total they individually provide the solutions required for final integration and usage of an entire system.

Routines and processes for developing and manufacturing prototype circuit boards has throughout the thesis stabilized to an acceptable and sufficient level, as described in Chapter 3 and 6. The following should be considered in the future though, including electronic design approaches:

- The concept of designing modular circuit boards should be discarded as an experimental mistake. Poor EMC and grounding results in problematic debugging and bad performance. All future designs should therefore be as integrated as possible to avoid further unnecessary problems. Essentially this means that as much electronics as possible should be included on a single circuit board. This will essentially improve EMC and grounding stability. Also, efficiency and probably performance will be boosted.

- The transition to integrated designs should also include the change from discrete components in 1206 packages to 0402 and 0603 packages, so that designs can be even more efficient by the higher degree of integration possible.

- The introduction of multi-layered circuit boards will improve the performance and functionality even more than the individual concept of integration does. Multi-layered boards will provide the ability to use low impedance ground and power planes, and also add the possibility for signal trace shielding. The degree of integration will also be increased, as components and traces can be places more freely in the design.

The work done here has placed a solid foundation for the development of the ultimate system for the SDTM. The remaining work to be done to reach this goal, using designs and solutions described in Chapter 6, can be divided into four main steps:

1. Manufacturing a first measurement setup for the SDTM sensor, only using a simple instrumentation amplifier design. When connected single-ended to the evaluation AD-converter circuit board available, this will work as a complete measurement platform for the project.

2. Integrating the SDTM or AAL002 sensor with a buffer pre-amplifier on a single circuit board. This will remove the need for transmitting small signals over coaxial or twisted cables, thus improving signal quality.

3. Miniaturize and integrate all signal processing and analog to digital conversion on a single circuit board. This will be the final evaluation step for the SDTM electronics. The system will give the ability to take a differential input and converting it to digital form on a single unit. The miniaturization can be done by using naked chips ordered from manufacturers, allowing a small and high performance design.

4. Designing a data acquisition system for the above, replacing the evaluation system currently used from Linear Technology. Because of high data rates and fast sampling speeds, this system will require implementation in FPGA, or similar technology. The use of integrated, high capacity memory will be required for local storage of measurements before transmission to a local computer or downlink system.

The requirements specifications described in Chapter 2 are intended for the sensor itself. When considering the electronic system, the requirements will change due to the limitations mainly present in the AD-converter and data acquisition systems. The following specifications will change when applied to the electronic system:

**Bandwidth** will be limited mainly by the Nyqvist frequency, and so by the AD-converter. The 125 MSPS ADC mentioned in Chapters 5 and 6 will thus set the bandwidth limitation to 60 MHz - far below the SDTM specification of 500 MHz. By using undersampling this 60 MHz bandwidth can be used in any frequnecy range allowed by the converter inputs. For example the range 440-500 MHz could be measured when aliasing is used.

In addition to the upper limit of the bandwidth, there will also be limitations to how far down in the spectra good measurements can be

done. The main limitation at lower frequencies will be the short sampling time of the AD-converter, since it must store all data on local memory. The amount of available memory will set the sampling time, and therefore the lower limit for measurable frequencies. The exact frequency will be set by the resolution. If the signal does not change more than the smallest resolvable step during the entire sampling time it cannot be measured.

**Resolution** is naturally set by the noise floor of the system, including all signal conditioning electronics. This means that a higher bandwidth will decrease the resolution. AD-converters with high resolution also tend to be slower than others. The resolution must be weighted against the sampling speed and therefore the bandwidth. The resolution is also limited by the total field range of the system. If a wider range is required, the resolution is automatically reduced.

If the intention of ÅSTC is to develop, manufacture and evaluate advanced and sensitive electronic systems in this and future project, the following improvements should be considered for the laboratory:

- A powerful and high bandwidth oscilloscope is a necessity in a research group with the ambition of further studying and developing electronics and other devices active in the RF spectra. This would, without doubt, be a necessary purchase to improve the laboratory considerably.
- A network/spectrum analyzer would naturally complement a powerful oscilloscope, but has to be weighted against the high cost of acquiring one.
- Acquiring a high frequency signal generator, powerful enough to output a sine wave exceeding, at least, 20 MHz.
- For digital measurements a high speed I/O interface card to one of the laboratory computers would be necessary. PCI-express cards with onboard memory of several gigabytes are available at speeds exceeding 100 Mbps for 24 parallel channels.
- A temperature regulated heating plate, preferably with a ceramic element to give optimal heating and cooling profiles.
- The introduction of multi-layer printed circuit boards should be considered for improvement of performance factors further.

## Final notes

The final product is intended to operate in space. This is the main future aspect of the entire project. Since the SDTM sensor is to be situated outside the spacecraft, to ensure a noise and interference free environment, it is critical that the electronics, including the sensors, are very durable to the ambient environment. Both particle and field radiation must be taken into account in the design. Temperature regulations will not be available, so the electronics must operate in a wide temperature range, without loosing too much performance. To avoid EMI coupling to the spacecraft body, the sensor should also be galvanically isolated from the main structure - no metallic booms or wires should be used if possible. The communication could instead be achieved using an optical link from the sensor to the main electronics, housed within the protected spacecraft body. Power supply can also be transmitted over an optical link using some kind of solar cells at the receiving end. If all this is to be possible, the sensor must contain a minimum of electronics and have extensive redundancy. Only the pre-amplification electronics should be in close proximity to the sensor, to isolate the signal and amplify just enough to reach the noise limitation of the system. All other electronics, such as amplifiers and data handling, should be protected by the main shields in the spacecraft structure.

There is still a lot of work to be done considering the electronics operability in the space environmenent. Although this report hasn't covered any aspects considering this, it has provided a solid understanding of the electronic and concepts required to achieve this goal. The important system designs have been investigated and concluded feasible.

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navId=H0,C1,C1155,C1001,C1150,P11912,D8577
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# Appendices

# Appendix A

# SDTM Requirements specification

The requirements specification document is the foundation throughout the work on a certain project. Here all performance and operating requirements are defined and described. Usually, the document refers to a specific mission, where the end product is thought to operate. The SDTM sensor doesn't have a mission decided for it yet, with the exception of the fact that it is supposed to be operational in a space environment. Still, there must be a foundation to refer the requirements to. For the SDTM, several previous and current space missons were studied during the requirements specification phase. Some of these derived requirements were already given in Chapter 2 but the complete set of data is found in Table **??**. The complete set of requirements are found in [2].

## Studied missions

**Rosetta**[1] will be the first spacecraft in history to follow and land on a comet during its way through or solar system. It will study, among other things, the physics of the comet, its composition and how it reacts to the increasing effects from the sun as it travels further into our solar system. The Rosetta orbiter uses two fluxgate magnetometers to study the interaction between the solar wind and the comet. The use of two sensors at different distances from the orbiter limits the influence of the self induced magnetic field through calibrations. The lander also uses a fluxgate sensor in combination with a plasma monitoring device to measure the small magnetic cavity created by the comet nucleus. The lander sensor must withstand extreme temperature variations on the comet surface.

[1] http://sci.esa.int/science-e/www/object/index.cfm?fobjectid=31445

Table A.1: Mission comparison for SDTM Requirements specification.

| | Noise at 1 Hz [pT/$\sqrt{Hz}$] | Noise at 10 Hz [pT/$\sqrt{Hz}$] | Resolution [pT] |
|---|---|---|---|
| Rosetta orbiter | 32 | 12 | 31 |
| Rosetta lander | 10 | | 10 |
| Cassini FGM | 3.9 | | 4.9 |
| Cassini OPM | | | 3.9 |
| Gallileo FGM | | | |
| Venus Express | 10 | | 8 |
| Cluster | 10 | | 7.5 |
| Themis FGM | 10 | 0.5 | 3 |
| Themis SC | 10 | | |
| SDTM target | 3.9 | 0.5 | 3 |
| | Range [$\mu$T] | Bandwidth [Hz] | Mass [kg] |
| Rosetta orbiter | 15 | 25 | 0.028[1] |
| Rosetta lander | 4 | 32 | |
| Cassini FGM | 44 | 30 | 8.82[2] |
| Cassini OPM | 0.256 | 10 | 8.82[2] |
| Gallileo FGM | 16 | | 7.2 |
| Venus Express | 0.26 | 128 | 2.8 |
| Cluster | 65 | 32 | 2.9 |
| Themis FGM | 25 | 64 | 1.54 |
| Themis SC | | 4000 | 2 |
| OAM | | 0.5E9 | |
| SDTM target | 65 | 0.5E9 | 0.02 |
| | Power [W] | Temp. range [°C] | Radiation dose [krad] |
| Rosetta orbiter | | -125/-45 | |
| Rosetta lander | | -160/120 | |
| Cassini FGM | 11.31[2] | -30/50 | 100 |
| Cassini OPM | | -10/40 | 100 |
| Gallileo FGM | 7.35 | -15/110 | 150 |
| Venus Express | 4.25 | -160/120 | |
| Cluster | 2.1 | -80/70[3] | 30 |
| Themis FGM | 0.85 | -35/25 | |
| Themis SC | 0.09 | | |
| SDTM target | 1 | -160/120 | 150 |

[1] without electronic box [2] both FGM and OPM [3] survival temperature is -130/90 °C

The **Cassini**[2] spacecraft mission is to travel to Saturn and land the Huygens lander on its moon Titan. During its mission it will study Saturn, its atmosphere, magnetosphere and the interactions with the interplanetary medium. Huygens mission is to study the composition of Titans atmosphere during its decent to the moon and analyzing samples of the surface. The Cassini orbiter carries a combined instrument including both a fluxgate and an optically pumped helium magnetometer. The combination of these sensors will give good measurements of the magnetic field.

The **Galileo**[3] spacecraft together with its atmospheric probe had as its mission to study Jupiter and its satellites. It succesufully did this and was in the end redirected into Jupiters atmosphere where it was destroyed. During its lifetime it made many discoveries and returned much information about the Jovian magnetosphere and atmosphere. It carried two fluxgate magnetometers placed on lightweight booms extending from the spacecraft.

The mission of **Venus Express**[4] is to study Venus and its physical properties. The main challenge with this mission is the high temperature variations found in the inner solar system - setting high requirements on the onboard instrumentation. The spacecraft carries the same dual fluxgate magnetometer as Rosetta and Mars Express. The sensor has high tolerance in temperature and has been proven reliable in previous missions.

**Cluster**[5] was launched in august 2000 and is still in operations. Its mission is to study the Earth's plasma environment, the dynamic interactions with the solar wind, tail dynamics and cross currents. For these tasks highly sensitive and reliable electromagnetic and particle instruments are required. Cluster uses an advanced fluxgate magnetometer to measure the magnetic field with high resolution and up to 67 samples per second. The fluxgate is mainly used to trigger other instruments upon events in the magnetic field. It also uses spatial-temporal analysis to measure the magnetic field and its cross-correlation with the electric field.

**Themis**[6] uses the constellation of five probes to study magnetic substorms and how they affect the creation and of auroras over northern America. Themis uses two magnetometers. The fluxgate is for measuring changes in the magnetospheric background during substorms. The search coil magnetometer is used to measure low frequency variations in three dimensions.

[2] http://saturn.jpl.nasa.gov/home/index.cfm
[3] http://www2.jpl.nasa.gov/galileo/
[4] http://www.esa.int/esaMI/Venus_Express/index.html
[5] http://sci.esa.int/science-e/www/area/index.cfm?fareaid=8
[6] http://www.nasa.gov/mission_pages/themis/spacecraft/index.html

**OAM** is a fictive mission [2] intended for studying the angular momentum of radio waves. Magnetoresistive sensors are well suited for such measurements and the SDTM bandwidth has therefore been extended to suit the fictive OAM mission.

# Appendix B

# ADS Tutorial

## Creating a project

A project should, as the name implies, contain all designs, simulations and circuit boards for an entire project. It is important to minimize the number of projects used. In the end, this will simplify your work considerably. Create a new design by choosing *File - New Project* in the main window, give it a name and press *OK*. A new window appears called *Schematic Wizard*, press *Cancel* or use the wizard if you need it.

## Creating a design

A new design is created from the ADS main window or from within any other design by choosing *File - New Design*. Each imported components and each single circuit or circuit board should be represented with a design, for simplicity and proper overview. Even parts of circuits can have their own designs. These can then hierarchically be imported as blocks in other designs.

## Making schematics of circuits

Drawing schematics in ADS is very simple. It basically consists of placing components and circuits and connect them with wires, as in any other electronic schematic software. All schematics are found in the subdirectory *Networks* in the ADS main window. This section will only describe the ADS schematic toolbars and the most important commands.

Figure B.1 shows the upper toolbar of ADS schematic. The more important functions are as follows:

17 is used if you have hierarchical blocks in your design. This button allows you to go into them and view their content. This can also be


Figure B.1: Upper toolbar in ADS Schematic.


Figure B.2: Lower toolbar in ADS Schematic.

done by right clicking the block.

18 does the same as 17, but moves you out of a block to see the hierarchy above it.

19-21 rotates and mirrors components or selections. Mirroring is done either horizontally or vertically. Rotation is used very often and can be done by pressing *CTRL-R* on your keyboard.

22 disables components and shorts any connections together.

23 disables components as well, but here connections are left open. Both 22 and 23 are frequently with discrete components such as resistors and capacitors.

Figure B.2 shows the lower toolbar of ADS schematic. The more important functions are as follows:

1 is the ADS internal component library. Choose a category here and the available components will be listed to the left of your schematic window.

3 is hierarchical connectors. Use these connections to connect to the hierarchy above. The connections don't update themselves in the higher hierarchy, so you have to delete and reinsert the circuit each time you change an internal-to-external connector.

4 is ground voltage reference connection.

8 is used to insert wires. This is used very frequently and is reached with the command *CTRL-W*.

9 is used to give your connections and wires (nodes) names. Do this by first choosing a name, and then pressing the node to assign the name to it.

10 runs the active simulation.

11 is used for tuning of circuit parameters. Choose a parameter in the dialogue that appears and the simulation will rerun each time you tune the parameter. This gives you the possibility to see how different value of resistors or capacitors will affect your circuit.

## Importing components

In addition to the large amount of components already included in ADS, it is possible to create components not available in the local library. There are two ways this can be done, either by creating a new design or by importing a simulation model, usually *SPICE* models, available from most manufacturers.

### Creating a component

The creation of a component will add this component to the local library, available to the entire project. To create a component for schematic purposes we do the following:

1. Create a new design from the ADS main window.
2. In the *New Schematic* window make sure *Schematic Wizard* is selected. Give your component a name and press *OK*.
3. In the wizard select *Circuit* and press *Next*
4. Choose the number of pins/ports your component will have. Make sure *Allow Symbol Selection* is selected, so that you later can make a symbol for the component. Press *Next*.
5. Identify each port with a name. The same name can't be used for two different ports. Select *Finish*. The wizard is now done.
6. The *Symbol Generator* opens.
7. Select if your component have pins on two (*Dual*) or four (*Quad*) sides. Select *Order Pins by Number* to get a counter clockwise orientation of your ports, as they are on a physical component. Click *OK* to generate a basic artwork.
8. You can now add graphics to the artwork with the available tools. When you are finished, save the design and close the window.
9. Your component is now available in the local library by selecting *Insert-Components-Component Library* in the schematic menu.

10. By opening the component design from the ADS main window you can now add internal electronics to the component so that it could work in a simulation.

If the component is to be used in a circuit board layout - you must create a *footprint* for the component. This is done as:

1. Even though we selected *Order Pins by Number* above, this is not reflected in the component schematic, only the artwork. Therefore we first must rearrange the order of the schematic ports to match the counter clockwise orientation we require. A good idea is to order the ports in the same way as they are place on the physical component, just as we did when we created the artwork.

2. When the rearranging is done, choose *Window-Layout* from the schematics window.

3. WARNING! When you are working with layouts - never click the command *Generate/Update Layout/Schematic* from the menu *Layout* or *Schematic*. Even though this command is useful and powerful in some cases, it usually creates total chaos.

4. In the layout window, draw the footprint of the component as described in data sheets. For detailed instructions on drawing - check the guide on drawing circuit boards later in this appendix.

5. When the footprint is done, go back to the schematic window and select *Place Components from Schem to Layout* in the menu *Layout*. Select a port and place it on its proper position in the layout. This port will now be mapped between the schematic and the layout, so that connections can be shown in both. When placing the ports in the layout it is important to make sure the attach right at the edge of the pad where traces should be connected. It is recommended to have the *Snap on Edge* and *Snap to Center* controls active when placing ports.

6. The component is ready to be used in layouts of bigger circuits. If you want to place the component in a circuit schematic to the layout, simply select *Place Components from Schem to Layout* in the menu *Layout*.

### Importing a simulation SPICE model component

If manufacturers have *SPICE* models available for the components used, these can be imported into a schematic and then used for simulation. Importing of *SPICE* models is done as follows:

1. WARNING! Text files containing *SPICE* models must be placed in a directory not containing special characters or spaces. It can only contain letters and numbers. This means you can't save the model on your computer desktop. Use for example C:/spice/ or similar. If you don't do this ADS will crash without warning and any chance of recovering lost work.

2. To avoid problems the *SPICE* import doesn't work if there are any open schematics, layouts or simulations. Choose *Save All* and *Close All* from the ADS main window before performing the import.

3. In the ADS main window choose *File-Import*

4. In the import window, choose to import *Netlist File* and where on your computer to find the text file containing the model.

5. Make sure *Input Netlist Dialect* is set to *PSPICE* under *More Options*.

6. Press *OK* to import. The component can now be found under *Networks* in the ADS main window.

7. If the component is to be used in a layout follow the description in the previous guide about creating component footprints.

## Simulations

### AC-simulation

An AC-simulation can easily be created in ADS by inserting the component *AC* from the category *Simulation-AC* into your schematic. In the options for the component you can choose start and stop frequency and step sizes. An AC-simulation will sweep all AC sources in your schematic that depend on the variable *freq*. The most common AC source is *V_AC*. The variable *freq* is built into ADS and used by many components. The results from this simulation tells you how the circuit behaves over a frequency range.

### Transient simulation

A transient simulation will show how a circuit behaves over time, with frequencies as they are set by the various sources. This is a good simulation to find problems considering unstable behaviour of your circuits. The simulation is created by inserting the component *Trans* from the category *Simulation-Transient*. This simulation will sweep the parameter *time*, that is also built into ADS.

### Plotting simulation results

When you run a simulation, either by pressing the button in the toolbar or by pressing F9, the plotting window will automatically open. Press any diagram you want to plot and an option dialogue appears after you have chosen where to place the graph. All the nodes you have given specific names can now be plotted. You can plot against the variable *time* or *freq* depending on what simulation was last run.

## Drawing circuit boards

Circuit drawing is basically about placing components and connecting them with routed traces. Even so, this takes a lot of effort and requires thorough planning and knowledge in electromagnetism, EMC/EMI and basic physics concerning circuit boards.

### General about drawing and layers

It is strongly recommended that each drawing is represented by a schematic. This will simplify routing and component placement very much, since connections between components will be visible in the drawing interface. Selecting *Artwork Type Synchronized* under *Design parameters* in the *File* menu ensures that layout and schematic connections stay synchronized at all times. So changes to connections in either view will show in the other. This is very useful, because the layout connections work with any geometrical figure. It is therefore easy to make a short circuit by misstake in the layout. But with synchronization these shorting connections will show up in the schematic and so are easily detected.

Layers are used to distinguish between different physical layers of the circuit board as well as other information and geometries that don't have any physical connection, such as support drawings and information text. It is important to use layers very distinct, to avoid problems when realizing physical circuit boards. The most used layers in ADS Layout are the following:

**cond** is the top conductive copper layer of a circuit board. All component footprints are placed in this layer and most routing of traces should be done in this layer as well.

**cond2** is the bottom conductive layer of a 2-layer circuit board. This layer should usually be left as an unbroken ground plane and should therefore not contain any traces, unless there is no other way.

**hole** is the layer containing all geometries that will be drilled through the circuit board. Vias, alignment holes, connectors and through hole components use this layer.

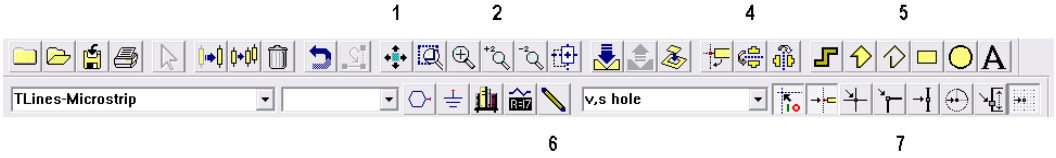


Figure B.3: Toolbar in ADS Layout.

Getting started with a new layout is very simple:

1. First make a schematic of the entire circuit.

2. In the schematic window choose *Window - Layout* from the menus.

3. Placing components from the schematic is done by selecting *Place Components from Schem to Layout* in the *Layout* menu. This requires that all components used in the schematic have proper layout information, such as footprints.

4. Use the tools available to route traces and draw other geometries in the layout to finalize the circuit board according to specifications.

The toolbar in ADS Layout is shown in Figure B.3 and the functions are as follows:

1 Zoom out automatically to show all geometries in the layout. Very useful tool.

2 Standard zooming tools

4 Rotating and mirroring. Remember that mirroring of components will give the result that the footprint no longer matches the correct orientation - this is very bad. So, never mirror components, only rotate them.

5 Geometry tools. Use these to draw the shapes you require.

6 Use this to route connecting copper traces between components.

7 Snap modes are very useful when routing and drawing to align with any other geometries, pins or grid coordinates. *Snap to Pin* is often required when making traces. This ensures that the trace end coordinates match with the pad. If not, the connection will not be valid and so not show up in the schematic.

Table B.1: Footprint dimensions for discrete packages when using R_Pad1 and C_Pad1 components in ADS [10]

| Package | Width (W) in mm | Separation (S) in mm | Length (L1) in mm |
|---|---|---|---|
| 1206 | 1.60 | 0.90 | 3.80 |
| 0805 | 1.30 | 0.70 | 2.60 |
| 0603 | 0.90 | 0.60 | 2.10 |
| 0402 | 0.60 | 0.50 | 0.75 |

### Through hole vias

Vias are used to connect one layer (cond) with another layer (cond2) by using drill holes through the board material. To remain the synchronization between layout and schematic, vias have to be included in the schematic. Do this by inserting the component *VIAFC* from the local library. Open the component options to select which layers are to be connected through the via. On two layer boards, these layers are the *cond* and *cond2* layers. Make the selection as follows:

- Cond1Layer = cond
- HoleLayer = hole
- Cond2Layer = cond2

The symbol of the via in schematic is a series inductor and resistor. It is important to connect each pin correctly, depending on which layer the connection is to be made. The following apply:

- Inductance pin = Cond1Layer
- Resistance pin = Cond2Layer

### Discrete components

Resistors and capacitors are discrete components, and they are used extensively in all designs. Any discrete component from the library could be used in ADS, as long as only schematic and simulations are used. For layout purposes, the components *R_Pad1* and *C_Pad1* are recommended. These components lets you set the dimension of their footprints. See Table B.1 for reflow soldering footprint dimensions on various discrete packages.

### Boolean logics

Boolean logics are used to make boolean operations between different layers. This can sometimes be very useful, for example when making text becoming

visible through a copper plane. This is done by making the following operation:

*cond* DIFF *text* ⇒ *cond*

If we at the same time choose to delete the original plane layer (cond), the text will become visible as cut outs in the new plane. There are endless possibilities with boolean logic and it could be used for almost anything. Playing around with it is recommended.

### Clearance and ground plane

Clearance is used to set a minimum of clear space between different geometries. It is a good way to make a ground plane or fill unused space of a board with copper. We do this as follows:

1. Draw a rectangle that entirely covers the whole layer where the plane is to be created. This will temporarily short all components and traces with each other.
2. Choose *Create Clearance* from the *Edit* menu. Select the rectangle you just draw when prompted to do so.
3. Select the layers from which the rectangle should be cleared. If you have drawn it in the *cond* layer you typically select the *cond* and *hole* layers.
4. Press *OK* and ADS clears the rectangle from the layers you selected.

## Exporting circuit boards for LPKF milling

To initiate the export choose *File-Export* from the layout window in ADS. A window appears where you can select the export format and save directory.

### Gerber 274X format

When milling out circuit boards in the LPKF mill, the format *Gerber* is used. After choosing this and pressing *OK* the exporting option window (*MTOOLS*) appears. The first time you export from a certain project you must chose the correct encoding by pressing the button *Translation Settings* and setting the *Gerber Output* to *RS274X*. Press *OK* to accept changes. ADS will now remember that *RS274X* is the default format, so you wont have to do it again for this project. In the *MTOOLS* window now select *Translate*. A new window appears where you can select what layers are to be exported - chose the ones you need, press *OK* and you are done. The file extension for *Gerber* is *.GBR*.

### NC-drill file format

Even though the *Gerber* format can be used for drill data, it is sometimes required to export this as a standard NC-drill file. This is done as follows:

1. First open the *Gerber* export window as described above. This has the title *MTOOLS*.

2. In the *MTOOLS* window select *Edit Apertures*. Press *Auto Flash*. ADS has now added a number of lines in the aperture list with the format *CMX_X*, with information that this is a circle (C), using metric dimensions (M) and size (X_X).

3. In the *Edit Apertures* window it is important to remember the *D-codes* for the dimensions of all holes that are used in the layout. Write these down. The *D-codes* will be used later. Press *Save*.

4. Chose *Translate* in the *MTOOLS* window. This will export your *Gerber* files.

5. When exporting is done, select *View Gerber*. The *GBRVU* window opens and shows all the exported *Gerber* data.

6. In the *GBRVU* window press *Aperture* to show tool information. As you can see there are no tools defined here.

7. Now use the *D-codes* that you have written down to identify what lines represent your drill holes. Manually insert the tool number, *Tool#*, and dimensions, *Drill Diamater*, for the drill holes used. The tool number can be any number, but it is recommended that you use the same number for a specific diameter in all designs. When you are done, press *OK*.

8. Now select *Tools-Drill-Excellon (Leading Zero Suppress)* from the menu in the *GBRVU* window. A list of NC-drill files for all your layers will appear.

9. Select your hole layer (usually *hole*) and press *Report*. Check that the correct number of holes are included in the report and that they have the correct diameter. Then close the report.

10. Press *OK* to export your NC-drill files. Note that there will be one file for each layer containing circles, but the only file that is to be used is the hole layer file. The file extension for *NC-drill* is *.DRL*.

# Appendix C

# LPKF and PCB Tutorial

This appendix describes the steps done for making circuit boards using the LPKF S62 ProtoMat circuit board plotter. Also described are the processes and routines for component placement, solder screening and reflow soldering used and partially developed during the thesis.

## LPKF preparation

The toolbar shown in Figure C.1 is from the program CircuitCAM. This software is used for preparation of exported circuit board drawings before milling. There are actually only five buttons frequently used in CircuitCAM, they have the following function:

1. Import drawing files.
2. Contour routing for cutting out.
3. Insert breakout tab in contour routing.
4. Rubout all layers - usually not used.
5. Insulate all layers. This translates the geometrical drawings to contour data.

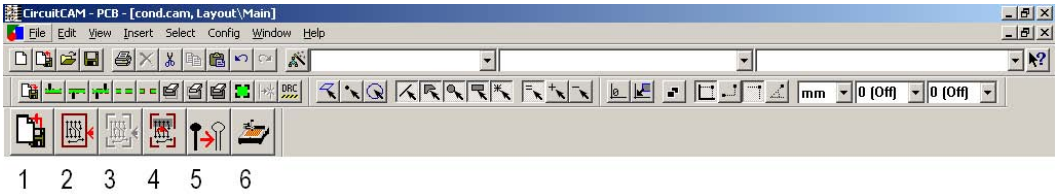


Figure C.1: Toolbar in CircuitCAM

6. Export LpkfCircuitBoardPlotter. Export to BoardMaster milling software.

Preparation work in CircuitCAM is easily done by following the steps below. Before using CircuitCAM, make sure drawings are exported correctly as described in Appendix B:

1. After having successfully created Gerber and NC-drill files as described in the previous tutorial the files are to be translated into control data for the LPKF mill. This is done by using CircuitCAM.

2. Before importing make sure that the tools to be used are inluded in the CircuitCAM template used. At IRF there is a Farid.CAT template that should be used. You can chose to create a new CircuitCAM project from a template in the *File-New* menu. The default template usually doesn't work.

3. In CircuitCAM use the "import" button to import your files. The following files needs to be inlcuded: Top Layer, Bottom Layer, Board Outline and drill data. The first three are in Gerber format and the drill data as an NC-file or Gerber. Mark all these files at once and chose import.

4. There will be one dialogue for each of your imported files. You have to choose the correct Layer internally for each of your files as follows, assuming your outline is in ADS default layer:

   - cond.gbr ⇒ GerberX TopLayer
   - cond2.gbr ⇒ GerberX BottomLayer
   - default.gbr ⇒ GerberX BoardOutline
   - hole.gbr ⇒ GerberX DrillUnplatted
   - hole.drl ⇒ NC-Drill DrillUnplatted

   For the Gerber files you leave all options untouched as this information in embedded in the file. For your NC-drill file, you have to choose the correct digits, check the preview before doing the import to see if it seems to be correct. This is because NC-files store float without any separator, the number 2.45 would be (digigts=2,3) 02450. If you haven't defined the digits in ADS, they are usally (2,3). Also make sure that units and decimal position match your file format. Always preview NC-data before importing!

5. When all your layers are imported and you have checked that they are correct it's time for contour routing. The contour routing will place

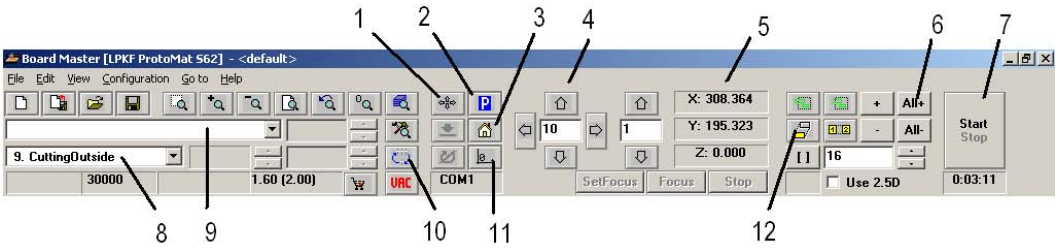


Figure C.2: Toolbar in BoardMaster

a broad cut-out around your circuit boards so that you don't have to cut them out by hand. Press the button Contour Routing, select your board outline layer, select *Outside* to cut outside this layer, then press OK. You can also choose how wide the cut should be and what tool should be used, but the default values are usually the best ones.

6. To avoid the boards from flying out when the are cut out you have to make breaks where the cutter wont cut. Do this by first making sure that only the contour routing is visible (View-Layers menu). Now place the marker near the point of your break so that a star appears in that point. Press Breakout Tab to make a break at this point. At least three breakout tabs should be used for each circuit board.

7. Press Insulate All Layers to prepare the data for exporting.

8. After making sure that the mill control software BoardMaster is running (see next section), press the button Export LpkfCircuitBoard-Plotter to export your files for milling. During this process, there are usually some error messages popping up, just pretend nothing has happened and press OK on them all.

## LPKF milling

The software for controlling the S62 circuit board plotter is BoardMaster. The toolbar for BoardMaster is found in Figure C.2, the marked buttons have the following functions:

1. Free move tool head by mouse to an arbitrary position.

2. Move the tool head to its parking position. This reveals the whole working area of the S62 plotter.

3. Move the tool head to its home position.

4. Incremental movement of the tool head in x/y directions. Units are in mm.
5. Current tool head position.
6. Add whole selected job to work phase.
7. Start milling selection.
8. Job selection.
9. Tool selection.
10. The toolbox shows inserted tools and tools required for current job. Also shows total distances for all of these.
11. Move the tool head to the reference position. This is the default position when the machine is switched OFF.
12. Manually move drawing on working area.

Once the work in CircuitCAM is complete, it is time to start using the BoardMaster program. The following should be done in BoardMaster to mill circuit boards:

1. After initially switching the S62 plotter ON, start the BoardMaster software.
2. When BoardMaster starts up, it will ask about tool status. If there is no tool in the mill head, just press OK. Otherwise, you must select what tool position is free before continuing.
3. To reveal the working area and available tools - press the *Parking* button to move the head to its parking position.
4. Before opening the hatch to the machine - press the *Open Toolbox* button, if not already there the head will move to its parking position. When the toolbox dialogue shows on the screen it is safe to open the hatch.
5. Place the circuit board material to be milled on the working area, separated by a cardboard cushion material. Use the alignment holes available both on the working area, the circuit board material and the cardboard to firmly attach the material. Tape should further be used to fasten the materials.
6. The 0.2 mm universal cutter used for almost all milling jobs, needs to be calibrated before starting the work phase. The calibration is done as follows:

(a) First use *Tool Selection* to select the 0.2 mm universal cutting tool.

(b) Move the tool with the *Free Move* or *Incremental Move* commands to a position the head where the cut is to begin. This should be a place that isn't used for other milling work later on.

(c) Use the manual free-move or incremental move commands to move the head to a position on the material that is not going to be used. On this position we will make a test cut.

(d) When in position press the *Tool Up/Down* button to move the tool closer to the surface.

(e) Before entering the material, make sure the tool is rotating by pressing *Start/Stop Tool Motor*.

(f) Enter the material by again pressing *Tool Up/Down*.

(g) Move the tool through the material with the movement commands to make a small cut.

(h) When done - press *Tool Up/Down* followed by *Start/Stop Tool Motor* to remove the tool from the material and stop the rotation of the tool.

(i) Press *Open Toolbox* to automatically remove the tool to its position and move the head to the parking position. If you only select parking, the tool will remain in the head. It is recommended to avoid having tools in the head when they are not used. If BoardMaster or the computer crashes, it will not remember if it has a tool in the head, which could be disastrous if not handled correctly.

(j) Open the hatch and use an appropriate measurement device to check the thickness of the cut. This should ideally be slightly more than 0.2 mm. About 0.21-0.22 is sufficient.

(k) If the cut is to shallow or too deep, repeat the calibration with a new cut.

7. When calibration is done, import the drawings from CircuitCAM as described previously.

8. Move the drawing to the right position on the working area, by selecting *Move Drawing* and then pressing and holding the mouse button on the drawing to move it.

9. You can visually check if your placement is within the board material limits, by moving the tool head to each corner of the drawing.

10. The milling and drilling is done in turns using job programs. The following should be used for a standard circuit board, in order of appearance:

(a) Marking Drills

(b) Drill Unplatted

(c) Milling Bottom

(d) Milling Top

(e) Cutting Outside

11. To initiate a job, select it from *Job Selection* and do the following:

    (a) Before starting the job choose *Open Toolbox*. The right side in the dialogue window shows what tools are used for the selected program and what distance the will travel. The left side shows what tools are available in the machine and the distance the have already done.

    (b) If any tools are missing for the current job phase, change them in both the list and the actual machine. Before removing any tools, make sure to write down their distances and manually entering the distances for the tools replacing them.

    (c) When the right tools are available for the job and non of them have passed their maximum distance, it is time to start the job phase.

    (d) To start the job - select the correct job from *Job Selection* press *All+* and finally *Start*.

    (e) The S62 circuit board plotter will now finish the current job according to the drawings provided.

12. repeat the above for the jobs *Marking Drills*, *Drill Unplatted* and *Milling Bottom*

13. When the bottom layer is done, choose *Milling Top* to see how the circuit board material is to be flipped in order to mill the top layer.

14. choose *Open Toolbox* before opening the machine and flipping the material.

15. When the material is in the correct position repeat the instructions above for the jobs *Milling Top* and *Cutting Outside*.

16. When all jobs are done - park the tool by selecting *Open Toolbox* again and remove the materials from the machine. The circuit boards are now cut out manually and finished.

17. Before leaving the machine, restore previous tools in the toolbox if you have used any others than the ones that were already there.

18. When you close BoardMaster the head returns to its reference position and moves the working area away - make sure not to leave anything on the working area when doing this.

19. When BoardMaster is closed, turn the S62 circuit board plotter OFF.

## Screening

For some packages, hand placing of solder paste is a terrible idea. An example is the 16 pin 3x3 mm QFN packages (LT1993-10). For these packages, solder paste screening is the best option. For this, stencils with the shape of the components footprints are used. These stencils can be ordered from manufacturers, but are very expensive. A better method is to use Kapton film and mill out a stencil with the LPKF mill. The thickness of the film should be about 100 $\mu$m to ensure the right amount of solder paste left on the board after screening. To make such a stencil we do the following:

1. Use a dummy layer and make rectangles over all pads in your drawing, that are to be included in the stencil. Then draw a rectangle in your stencil layer over the whole board.

2. Use boolean logics to invert the footprints through the stencil layer, so that you have a layer that covers the entire board, with the exception of footprints, that now should be left as open cut-outs.

3. Export this layer to Gerber format.

4. Do the normal CircuitCAM procedures previously described to get the stencil layer and the outline layer into the LPKF BoardMaster software.

5. In BoardMaster, make sure the 0.15 mm straight mill is used instead of the universal cutter selected by default.

6. After firmly attaching the film in the LPKF make sure that the mill doesn't mark the outline when milling. This will cause the Kapton film to fly away and get damaged. This can be done by manually selecting what parts of the current layer that is to be milled out.

7. The final stencil/film must be processed further after this. Etching and cleaning is required to make edges straight and clean from remains after the milling work.

8. When screening to the circuit board make sure that the film is fastened at only one end, so that it can be removed without messing up the solder paste.

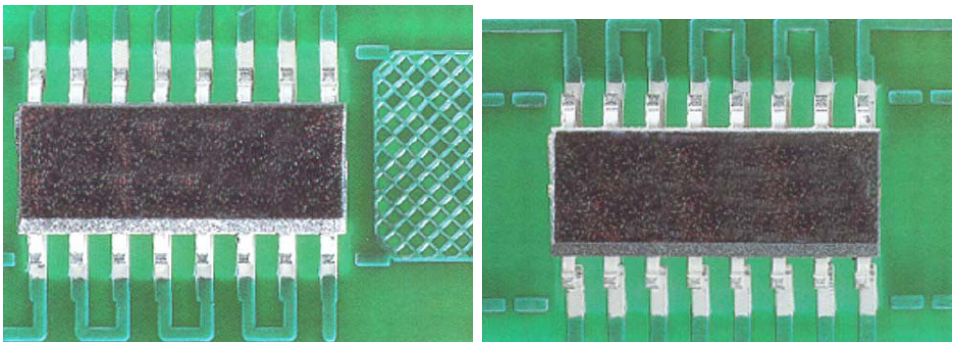

Figure C.3: Examples of good and acceptable placement. Both should function properly. Source: [10].

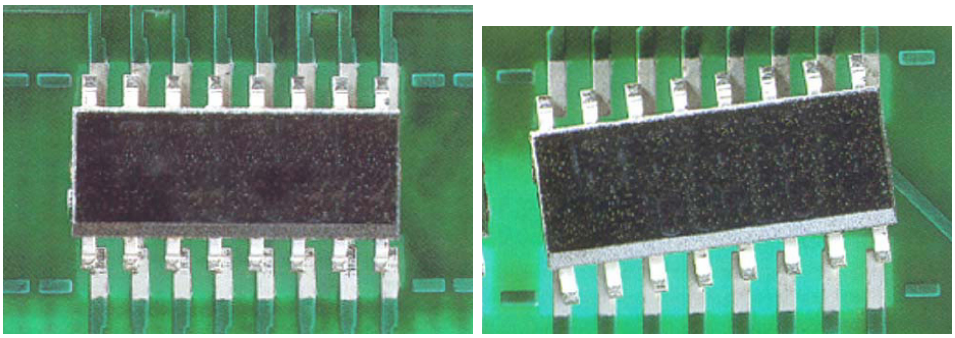

Figure C.4: Examples of bad and really bad placement work. Both will require rework to guarantee proper function. Source [10].

9. If the board and film have alignment holes use these to get the right alignment. Otherwise it is no problem to align under a microscope and tape the film to the board (the film must then be slightly smaller than the board).

10. Screening should be done in one direction - away from the fastened end. Make sure you have enough solder paste so that you don't have to repeat the movement more than once or twice. Too many movements or movement in the wrong direction will result in alignment changes and give a mess. Acceptable displacement is 0.1 to 0.2 mm depending on pad size.

## Placing

Small surface mount packages are usually not placed by hand. Instead a pick-and-place machine is used. The machine uses a vacuum to lift components with a needle. The vacuum is turned on and off each time you put upwards

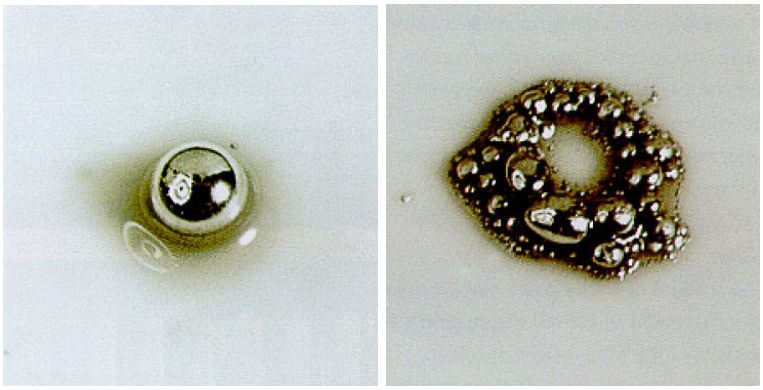

Figure C.5: Two examples of solder balls. Left is a good single ball. Right is a bad soldering result and requires rework. The bad result is because of prolonged heating or too high temperatures. Source: [10].

pressure on the needle, that is when you pick up the components and when you place them on the board. Accurate placement is achieved with a tilted microscope, so that you see the board and components magnified and slightly from the side. It is important to remember NOT to accidently place the needle near or in your solder paste - this can damage the vacuum system.

The accuracy of placement is not as important as one could think. A rule of thumb is that the component pin should cover no less than 75% of its pad. Most packages will align themselves due to surface tension once the solder paste on the pads are heated. A good reference in the subject of soldering and placement is found in [10]. A few examples are found in Figures C.3 and C.4.

## Soldering

There are two main methods for soldering surface mount components, reflow soldering and wave soldering. Wave soldering is common in the industry and often used for mass production, where the whole manufacturing process is automated [10]. Reflow soldering is usually the final stage of the processes described in this tutorial, beginning with stencil screening and component placement. Reflow soldering is recommended to follow the heating profile illustrated in Figure C.6. The figure contains the following steps:

**Preheating** is the initial step of the process. The increasing rate should not exceed 10 °C/s to avoid the solder paste from spattering.

**Equalization** is the longest period of reflow soldering. Here we make certain that all solder paste has the same temperature before melting it. This is because larger components with more solder paste would otherwise

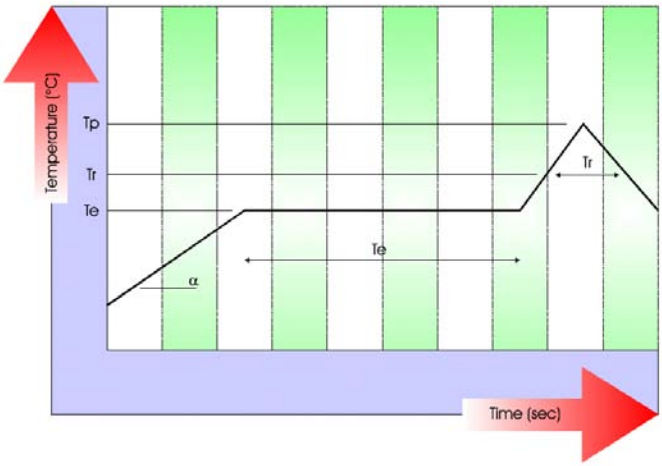


Figure C.6: A typical Reflow heating profile. Source: [10].

not solder entirely. Smaller components with less solder paste could end up as in Figure C.5 while waiting for larger components to solder. The temperature in this stage should not exceed 160 °C and the time should be 1-5 minutes. Less time is better, as the solder paste can degrade of prolonged high temperatures.

**Reflow** is the melting phase. Here it is only required to reach a certain temperature. For standard solder paste a temperature of 213 °C is required for proper soldering. The maximum temperature of a standard epoxy glass circuit board is 280 °C. Time above melting temperature should not exceed 1 minute.

**Cooling** is the final period. It should be a controlled descend, not to fast, not to slow. A few minutes to room temperature should do the trick.

The process is usually done in an infrared or convection oven. In the ÅSTC laboratory, no good enough oven was available, instead a hot plate was used. On top of the plate a big metal block was placed with a thermometer inserted into the material. The block makes sure heating rates are kept within limits and simplifies the equalization phase, as the block can stay at a more or less constant temperature even with the plate switched off. The plate did not have any temperature regulation, so as to follow the profile in Figure C.6, the temperature had to be controlled manually with the thermometer as follows:

1. The plate should start with full power, until the thermometer shows about 120 °C. The temperature will then equalize to about 160 °, where it should be left for a little while.

2. When your stomach tells you the temperature has equalized enough, put full power on again until the temperature reaches about 200 °C and then switch it off.

3. Make sure visually that all components have melted properly. If you feel that this hasn't happened, use a hot air pistol to give parts of your board i final push to melting.

4. When melting is complete remove the circuit board from the plate and place it somewhere where it wont cool too fast, for example something non metallic.

## Finalizing

After soldering the circuit board should be inspected under a microscope to visually confirm that all components have soldered properly. Through hole vias, various connectors and hole mounted components are then manually soldered to the board. Vias are easiest done by cutting off resistor legs and use them to connect the top and bottom layer of the board. Such vias require 0.6 mm diameter of vias holes.